The effect of Nickel barrier plating thickness in solderability of Iron (Fe) based leadframe

Edgardo P. Morales Jr.
Marie Crisse L. Lee
Christian Paul C. Maliksi

Process Engineering Department, QA FA/Reliability Department
Excelitas Technologies Philippines, Inc., LISP I, Diezmo, Cabuyao, Laguna
Edgardo.Morales@excelitas.com, Maket.Lee@excelitas.com, ChristianPaul.Maliksi@excelitas.com

ABSTRACT

Fe-based leadframes are used in the semiconductor industry because of their good coefficient of thermal expansion match to silicon, excellent mechanical strength and lower cost compared to copper-based leadframes. They also exhibit excellent thermal dissipation properties, making them ideal for power, automotive and other high current devices. They are, however, prone to oxidation and corrosion and exhibit poor bondability. Thus, they are normally plated with layers of copper, nickel and silver,
This study investigates the importance of a Nickel diffusion barrier for leadframes to avoid exposed Cu and Fe, leading to corrosion, oxidation, and solderability issues. Metallurgical analysis of the equivalent metal layers and intermetallic through Scanning Electron Microscopy with Energy Dispersive X-ray Spectroscopy (SEM- EDX) was done on samples with plating layers of the Ni diffusion barrier (<2 µinch) and with improved plating thickness of diffusion barrier (≥10 µinch). The sample with higher diffusion barrier thickness shows remaining 25.55 microinch Ni diffusion barrier thickness while sample with less diffusion barrier having no Ni diffusion barrier left. Cu formed intermetallic compound (IMC) with tin were observed on this sample. This IMC is brittle and has shown Kirkendall voids formation which correlates to lower push test.

1. 0 INTRODUCTION

In semiconductor packaging, the leadframe is an essential component for providing electrical and mechanical support for the integrated component (IC). Even after the introduction of other technologies such as Chip scale packaging, substrate base packaging, and wafer level packaging, leadframes remain an important part due to cost-effectivity and high-volume production capabilities [1]. A lead frame such as those used for light emitting diodes (LED) standing lead frame design utilizes base metal such as Iron (Fe) and Copper (Cu) due to its lower cost yet has good formability which is best for stamping process, rigid and high strength, and stability. Although Fe is inferior to Cu in terms of electrical conductivity its cost effectiveness and higher tensile strength make it an option to some manufacturers while compensating the downside by introducing plating layers such as Cu. Since the Cu used as a plating layer is limited to a few microinches, the cost is still comparably lower than using Cu as base metal [2]. The copper layer enhances the thermal and electrical conductivity of the Fe-based leadframes. In the late 1970's base metal are being directly plated with the selected top plating, until the Ni diffusion barrier was introduced in early 1980's [3]. The diffusion barrier is used to prevent the migration of the inner layer to the outer layer such as Fe and Cu to the metal surface, resulting in oxidation and corrosion [4]. Another issue that the diffusion barrier addressed is the formation of IMC between Cu and Ag (CuAg, Cu_3Ag) and Cu and Sn (Cu_6Sn_5, Cu_3Sn). Controlling the growth of these IMC is important especially when thermal stress is involved such as Oven Curing, reflow, and solder dipping. The resulting IMC is generally harder and more brittle than the parent metal (Cu, Sn, and Ag). Most commonly use diffusion barrier is Nickel (Ni) since aside from preventing the diffusion, it also provides strong mechanical bond to most commonly use base metal (Fe, and Cu) and top plating (Ag, Au, and Sn) [5]. The top plating of Ag provides the leadframe with good bondability, protection from oxidation, enhances solderability, improve electrical and thermal conductivity and for LED devices it also improves reflectivity. [4]

The Solder Dipping process is one of the processes that can induce and accelerate IMC growth. In the process, leadframe is dipped into the molten solder typically at 260 °C – 300 °C to provide solderable coating which is convenient during mounting or soldering of the components to boards. The solder used is Tin (Sn) and reacts with layer metal Copper (Cu) to form a good metallurgical bond. The IMC further grows depending

on the additional thermal exposure the device experiences. A Ni diffusion barrier can be introduced to control this growth. Ni, however, can also be consumed during the process depending on its thickness as well as exposure time to solder dipping temperatures.

A customer complaint of a lower push-test for the new IRED lead frame relative to old lead frame has been received.
The push-test is performed by clamping the PCB while pushing the LED component downward till the component breaks away from the PCB. A simple illustration was shown in Fig 1. The resulting force reading obtained from the affected LED component (C1) was compared to another unaffected LED component (G1) which is also supplied by our company and shows significant difference in performance shown in Fig 2.

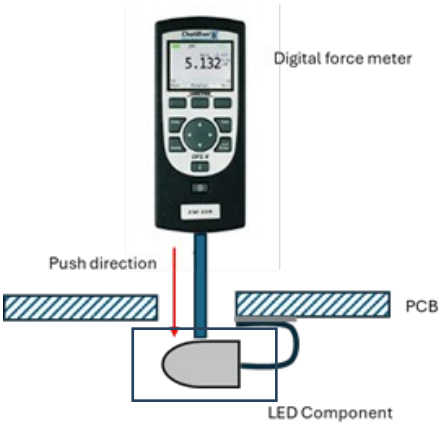

Fig 1. Push-test illustration

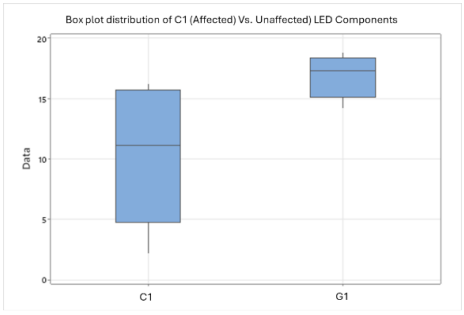

Fig 2. Push-test distribution of C1 (affected) and G1 (unaffected) LED components (in kg-f)

This study will investigate how the Nickel-plating thickness affects the occurrence of Kirkendall voids and the push-test that affects solderability.

2. 0 REVIEW OF RELATED WORK

Nickel is widely used as a diffusion barrier between copper leadframes and solder joints. In a Study [5] Nickel was proven to have slow diffusion rate to Sn preventing the formation of IMC growth specially Cu-SN intermetallic. In another study titled [4], it was demonstrated that without Ni diffusion barrier the diffusion of Cu to Ag continues as exposed to thermal stress, same as IMC growth responds to thermal exposure. While in a study conducted by Chia, P. [6], shows that <70 nm (<2.75 microinch) Ni barrier in Cu/Ni/Sn nanoscale multilayers is prone to rapid depletion during soldering or thermal aging, leading to accelerated Cu-Sn IMC formation, increased Cu_3Sn phase, and void formation. Maintaining Ni thickness at or above 70 nm (>2.75 µinch) is critical to stabilize IMC phases, reduce voids, and improve interconnect reliability.

3.0 METHODOLOGY

The following materials and techniques were used to analyze and compare sample leadframes in this study having different Ni Diffusion barrier thickness.

3.1 Materials

Steel Plate Cold-rolled Commercial (SPCC) – a specific grade of cold rolled carbon steel defined under the Japanese Industrial standard JIS G314. It is the raw material for the base metal of the leadframe in this study which is commonly used for this application due to its consistent quality, formability, and suitability for mass production of stamped and formed components such as leadframes [7]

These raw materials are stamped to create the leadframe and then plated with Cu (Copper), Ni (Nickel), and Ag (Silver).
Samples have different Ni Barrier thickness which is the sample with less plating thickness of diffusion barrier (<2 µinch) C1 LF and with improved plating thickness of diffusion barrier (≥10 µinch) C2 LF. C2 LF Ni plating thickness is based on the other unaffected LED components
(G1) which also has high push-test results.

3.2 Metallurgical Analysis

Scanning Electron Microscopy – Energy Dispersive X-ray Spectroscopy (SEM-EDX) was used to identify, measure and to analyze the plating/intermetallic layers of the leadframes.

3.3. Validation

The supplier was requested to increase the minimum plating thickness of the Ni from <2µinch to 10µ≥inch. The leadframe with improved plating thickness (≥10 µinch) was processed and subjected to cross sectional SEM EDX to check the response of thicker Ni Diffusion barrier and compared to leadframe with very thin Ni layer (<2 µinch). Push -test will be performed to check its correlation to the root cause as required by the customer.

4.0 RESULTS AND DISCUSSION

4.1 intermetallic Formation

Intermetallic compounds form when two unlike metals diffuse into one another creating species materials which are combinations of the two materials [8]. Intermetallic growth is the result of the diffusion of one material into another via crystal vacancies made available by defects, contamination, impurities, grain boundaries and mechanical stress [8]. The growth of the intermetallic layer is diffusion controlled and follows a parabolic growth curve expressed in below equation:

[8]

Where X is the intermetallic layer thickness, t is time and k is growth constant at specific temperature which is express in below equation:

[8]

where:

- is a pre-exponential factor,
- E is the activation energy for diffusion,
- K is Boltzmann constant,
- *T* is the absolute temperature in Kelvin

The intermetallic growth rate slows down over time due to increasing diffusion path length making it harder for the atoms to diffuse through the growing intermetallic. This growth rate is highly accelerated by temperature.

Ag and Sn IMC

Ag diffusion to Sn is relatively the fastest among the layers of the sample lead frames [9] and the resulting IMC is primarily Ag_3Sn which is ductile and mechanically robust microstructure [10][11].

Cu and Sn IMC

Cu and Sn diffusion is fast and the Cu3Sn and Cu6Sn5 are typically brittle and may be susceptible to crack growth [12]. These intermetallic are also non-solderable and partially solderable, respectively.

Ni and Sn IMC

Ni and Sn interdiffusion is relatively slow resulting in much thinner intermetallic compound (IMC) layers compared to Cu and Sn IMC [13]. The primary IMC formed is Ni_3Sn_4 which is hard but more brittle than Cu and Sn IMCs. Despite the brittleness, it enhances the overall strength of solder joints and provides a stable, adherent interface [14]. It is also less prone to excessive growth compared to Cu-Sn IMCs, which helps maintain joint reliability over time [15].

4.2. Evaluation of Potential Root Cause

From the result of Root cause analysis by elimination of several factors the very thin Ni barrier was identified as the most probable root cause. The effect of processes such as solder dip which is part of the process shown in Fig 3. may yield to depletion of the thin Ni layer and form Cu-Sn IMC which varies depending on the exposure to high temperatures and can associate Kirkendall voids and exposed Cu.

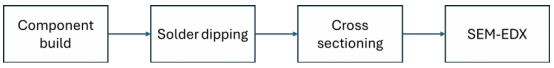

Fig 3. Process flow

4.3. Plating layers after solder dip

The original plating layers are shown in Fig 4 (left side). The first layer Silver (Ag) will dissolve in the molten Tin (Sn) after the 3 seconds dipping being highly solderable metal forming Ag_3Sn Intermetallic compound (IMC). This reaction was shown in Fig 5 result where Sn is observed in the top layer instead of Ag. The Ni layer serves as a barrier to prevent direct diffusion of Cu to Sn. If there is no Ni barrier, Cu diffuse into Sn and an intermetallic compound (IMC) will form Cu3Sn and Cu6Sn5 which are typically brittle and may be susceptible to crack growth [12].

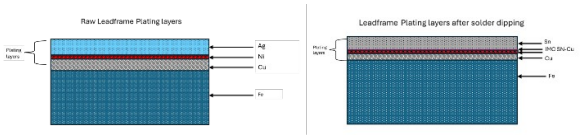

Fig 4. Plating layers before and after Solder dip

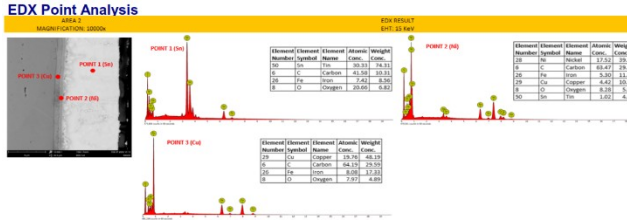

Fig 5. SEM EDX result plating layers

The result of cross section SEM-EDX show plating layers of ≥10 µinch Ni layer compared to leadframe with <2 µinch is shown in Fig 6. The leadframe with improve Ni layer thickness has Ni layers of 25.55 µinch Ni while the leadframe with thin layer Ni has no Ni layer after the test. Thus, it shows that the thin layer was depleted after the solder dip process while the improve Ni layer was not fully depleted. Based on the SEM-EDX results, an intermetallic was formed at point 2 which reflects the Ni-heavy region but with a presence of Sn.

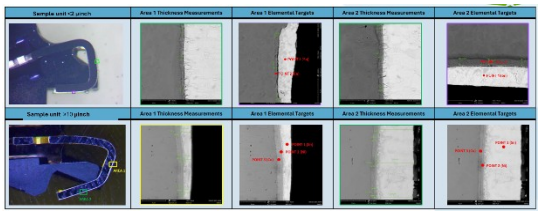

Fig 6. SEM EDX result plating layers comparison

4.4. Kirkendall voids

Kirkendall voids are formed because of Kirkendall effect which is due to unequal diffusion rates of atoms in diffusion couple. The formation involves several steps such as unequal atomic diffusion rate, vacancy flux and accumulation, nucleation of voids, void growth, and microstructural effect. In the sample leadframe layers, the diffusion rate was previously discussed, and Cu to Sn diffusion rate is fast making it prone to Kirkendall effect. Kirkendall voids act as stress raisers and initiation points for mechanical crack formation. During the process of solder dipping, which is heated up to 270 ºC the fast atomic diffusion of Cu to Sn creates an imbalance atomic flux at the Cu3Sn/Cu interface [18]. One way to visualize this is people migrating from provinces to cities. Those in the province which represent the Cu atoms tends to migrate to the city representing the Sn side, which is due to more available jobs and convenient living in the city representing the thermal energy(heat), while there are lesser people migrating to province, which causes population imbalances resulting to lesser houses and facilities in the province which represent the voids as a result. Conversely the slower diffusion rate of Ni to Sn is the opposite of Cu to Sn diffusion rate. This is like the improving province having more available jobs representing the slower kinetics and growth coefficient in the intermetallic and growth constant formula, resulting to lesser people migrating to the city representing the Sn Side. Although the imbalance can still form Kirkendall voids another factor such as the thickness of IMC form is relatively thin and the slow diffusion rate tends to result in a less severe vacancy flux imbalance [19].

The Sample unit ≥10 µinch Ni has no long Kirkendall voids compared to Sample unit <2 µinch Ni with observed long Kirkendall voids as shown in Fig. 7.

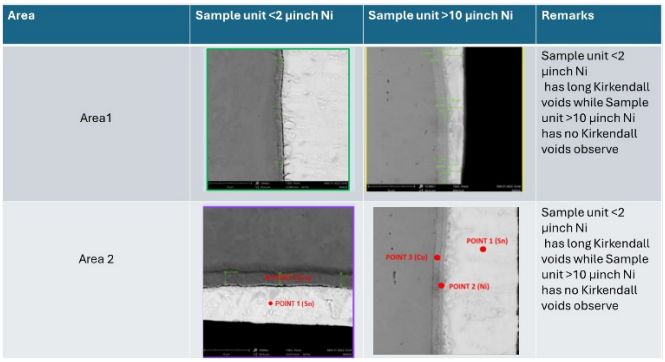

Fig 7. SEM EDX result Kirkendall voids

4.5. Push test result:

The push- test result in Fig 8. shows that the leadframe with very thin Ni plating thickness (C1 LF) has low push test with mean 5 kg-f while (C2 LF) improve Ni plating thickness has mean of 11 kg-f push test results. The C2 LF push-test result is comparable with G1 LF result (refer to Fig. 3)

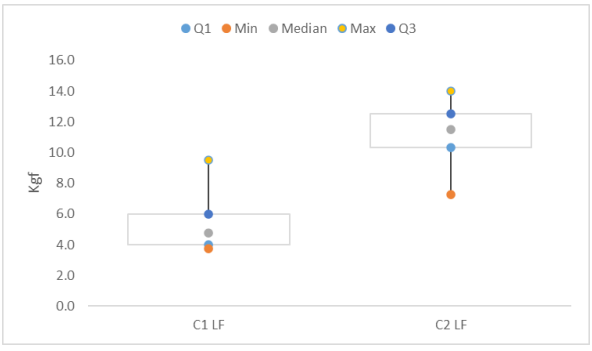

Fig 8. Box plot distribution C1 LF (<2 µinch Ni) and C2 LF (≥10 µinch Ni)

5.0 CONCLUSION

Improving the plating thickness of Ni Barrier will prevent its total depletion of during solder dipping process which will avoid the formation of Cu-Sn IMC as well as large Kirkendall voids. A sufficient layer of Ni barrier thickness contributes to the reliability of the solder joint. Push- test result correlates to the improvement in Ni plating thickness having higher push-test result for high plating thickness.

6.0 RECOMMENDATIONS

The minimum Ni plating thickness specification will be adjusted to ≥10µinch, while sustaining the solder dipping time of 3 seconds.

7.0 ACKNOWLEDGMENT

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9.0 ABOUT THE AUTHORS

Edgardo Morales Jr. is an Engineer II from Process Engineering Department in Excelitas Technologies Phils. Inc. and is part of the HeNe engineering team. He has a BS degree in Electronics and 8 years of supervisory experience in semiconductor manufacturing companies.

Marie Crisse Lee is a Unit Manager in Process Engineering Department in Excelitas Technologies Phils. Inc. who spearheaded the HeNe engineering team when it was transferred to Excelitas Philippines from an overseas site. She has a BS degree in Electronics and 13 years of process engineering experience.

Christian Paul C. Maliksi is a Senior Engineer I in QA Department in Excelitas Technologies Phils. Inc. He has a BS degree in Materials Engineering and 10 years of experience in Quality Assurance focused on Failure Analysis and Reliability.