DEFINING THE MINIMUM RETEST INTERVAL AT AMBIENT TEMPERATURE FOR RELIABLE FINAL TEST RESULTS IN GAN DEVICES

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ABSTRACT

A major challenge with Gallium Nitride (GaN) products is their susceptibility to inherent trapping. Charge trapping can lead to current collapse, voltage drift or low power output which can negatively impact linearity of the device and worsen EVM (error vector magnitude) in application.

It also affects the repeatability test in production run thus a 24-hour retest waiting time was introduced which showed significant recovery in GAN electrical performance. However, given the growing demand for GaN devices, this is not practical in the production environment.

The study was conducted to assess whether the current 24-hour minimum waiting time is still valid and identify the shortest possible waiting time that still ensures accurate electrical performance.

The assessment used retest intervals of 6, 12, and 24 hours at ambient temperature. Sample sizes ranged from 30 to 165 from different products with various diffusions to assess the trapping recovery. Yield and electrical performance were analyzed using the Two-Proportion Test and One-Way Analysis of Variance (ANOVA).

With a minimum retest interval of 6 hours, no statistically significant impact on yield ($p = 0.41$) and electrical performance ($p = 0.06 – 0.98$).

1. 0 INTRODUCTION

The advantages of GaN transistors include higher breakdown voltage, power density and thermal conductivity, and reduced power requirements which are beneficial for RF Power applications. However, it is also known that GaN is affected by many types of trapping such as different trapping locations, different energy levels and temperature.

The GaN trapping effect refers to the behavior of traps in Gallium Nitride (GaN) devices, which can capture and release electrons or holes, leading to charge accumulation and affecting device performance.[1]

GaN devices suffer from charge trapping. This acts as a lagging effect (short term, micro to milli seconds) and a memory effect (longer term, hours).[2]

The lagging effect causes problems in the application affecting EVM while the memory effect makes retest in the same run non-repeatable (in production, qualification, and Measurement System Comparison tests).[2]

Experiments with different retest intervals were performed previously (old GaN types) which showed recovery of leakage parameter vs waiting time (hours). Fig. 1 shows that after a 0.5-hour delay, minimal recovery was observed but with a 24-hour delay significant recovery was seen.[3]

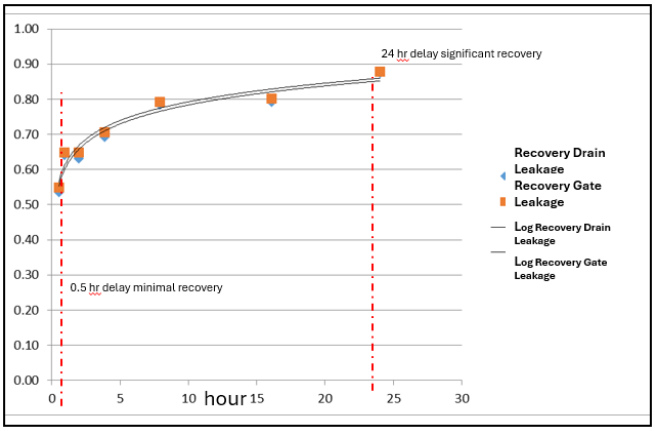

Fig. 1. Waiting Time Experiment: Recovery Rate per Waiting Interval.

Thus, to keep the impact of trapping within an acceptable range, the standard approach for GaN DC Final Test is 24

hours minimum waiting time prior doing retest. This is not practical for production, especially with the high-volume demand of GaN.

A study was done to verify if a minimum waiting time of 24 hours is still required and to determine the shortest waiting time that gives accurate results, using released DFN GaN and ACP GaN types of the same technology.

2. 0 REVIEW OF RELATED WORK

Trapping effects represent one of the most critical reliability challenges in Gallium Nitride devices, significantly impacting their long-term performance. These effects arise from defects in various regions of the device, including the surface, buffer layer, and bulk material. By traps, we mean energy states that exist within the bandgap due to lattice imperfections or contamination. These traps can capture and release charge carriers during device operation and reduce the highly conductive properties of the device. This dynamic process disrupts the steady-state charge distribution and electrical field within the device, leading to issues such as threshold voltage VTH instability, increased dynamic on-resistance (RON), and reduced current-carrying capability.[4]

Surface traps, commonly caused by dangling bonds or adsorbed contaminants at the AlGaN/GaN interface are particularly detrimental in high-electron-mobility transistors (HEMTs). These traps can interfere with the two-dimensional electron gas that forms at the interface, reducing electron mobility and degrading switching performance. Under continuous high-voltage operation, surface traps will accumulate charge, leading to field redistribution and undesirable transient effects.[4]

Buffer layer traps are another major concern in GaN devices. These are typically associated with defects in the GaN or AlN buffer layers, such as threading dislocations or vacancies. During high-stress operation, these traps can capture electrons, altering the electric field distribution and increasing the device's dynamic RON. This phenomenon, known as dynamic RON, is particularly problematic in power switching applications where extremely high efficiency and fast switching speeds are critical.[4]

These significant impacts on electrical performance due to trapping demanded that GaN devices be retested after a certain interval which was initially set to 24 hours. Therefore, in the study, different intervals were evaluated to define the shortest possible waiting time ensuring that the electrical performance of GaN devices remains reliable during retest.

3.0 METHODOLOGY

The study investigated the minimum retest waiting time to ensure consistent performance of DC parameters: drain leakage, gate leakage and threshold voltage, which are critical indicators of charge trapping behavior in GaN products.

3.1 Material Selection

For the selection of materials, factors that might affect trapping were considered such as different diffusions and the type of products. Two package types were used: DFN and ACP GaN with 165 and 30 samples selected, respectively. Samples selected (good and reject units) coming from >=10 different diffusion types.

3.2 Procedure

Waiting time interval will be 0 hr, 6 hr, 12 hr and 24 hr (see Fig. 2) at ambient temperature only using same tester, test program, and test circuit.

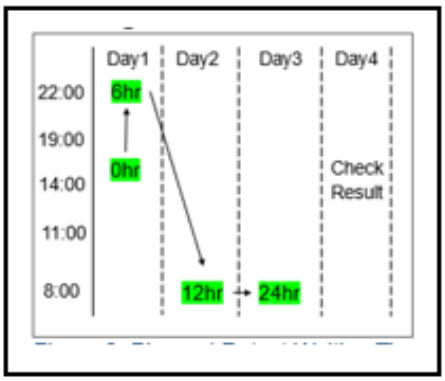

Fig. 2. Planned Retest Waiting Time.

The sample sets for different waiting time interval prior retest are summarized in Table 1.

Table 1. Samples and Waiting Time Interval

Package Type	# of Samples	# of Diffusion	Waiting Time Interval at ambient temperatur
DFN GaN	165	15	0hr, 6hr, 12hr, 24hr
ACP GaN	50	13	0hr, 6hr, 12hr, 24hr

3.3 Method of Analysis

A Two-Proportions test and one-way ANOVA were conducted to determine whether shorter retest waiting time

interval had a statistically significant impact on yield and key electrical parameters.

4.0 RESULTS AND DISCUSSION

This section presents the minimum retest waiting time interval in DC that maintains accurate results.

Samples from different waiting time intervals were assessed using the same test recipe and hardware. Data were grouped together by waiting time to create a single test event per test occasion for easier interpretation using Statistical tools. See Tables 2 and 3.

Table 2. DFN: Waiting Time, Quantity and Yield

Retest Waiting Time Interval	Qty	Yield (%)
0 hour	165	36.4
6 hour	165	38.2
12 hour	165	38.2
24 hour	165	39.4

Table 3. ACP: Waiting Time, Quantity and Yield

Retest Waiting Time Interval	Qty	Yield (%)
0 hour	30	86.67
6 hour	30	86.67
12 hour	30	86.67
24 hour	30	86.67

As seen on Table 3, ACP GaN Type showed equal yield for all intervals. For DFN GaN type, statistically comparable yield among 6, 12 and 24 hours (p=0.411) as shown in Fig. 3 using the Two-Proportions Test.

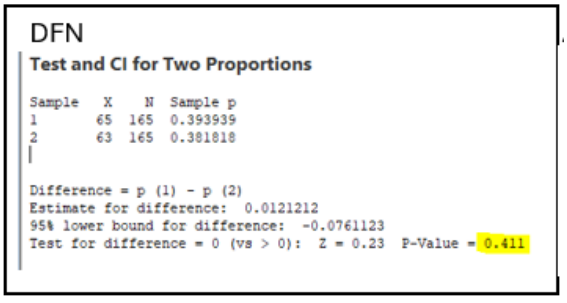

Fig. 3. Two-Proportions Test 24 hr. vs 6/12hr.

For the DC parameters—drain leakage, gate leakage, and threshold voltage—the responses at reduced retest intervals of 6 and 12 hours were statistically comparable to those at 24 hours for both DFN GaN and ACP GaN packages, as shown in Figs. 4 and 5.

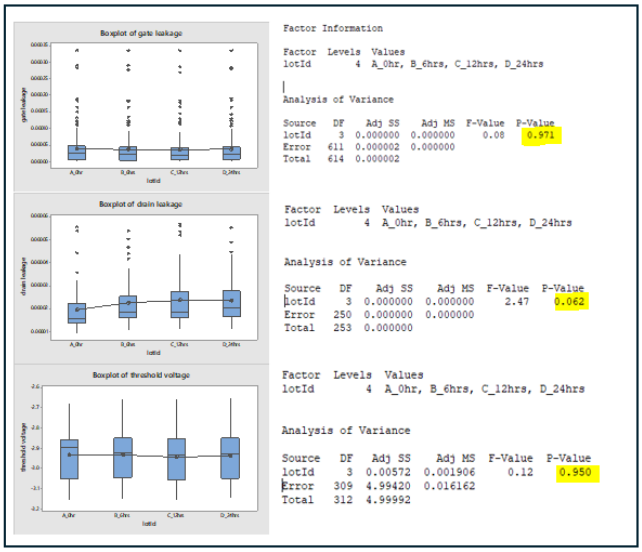

Fig. 4. One way ANOVA (Box plot representation) for DFN GaN on different waiting time intervals for retest.

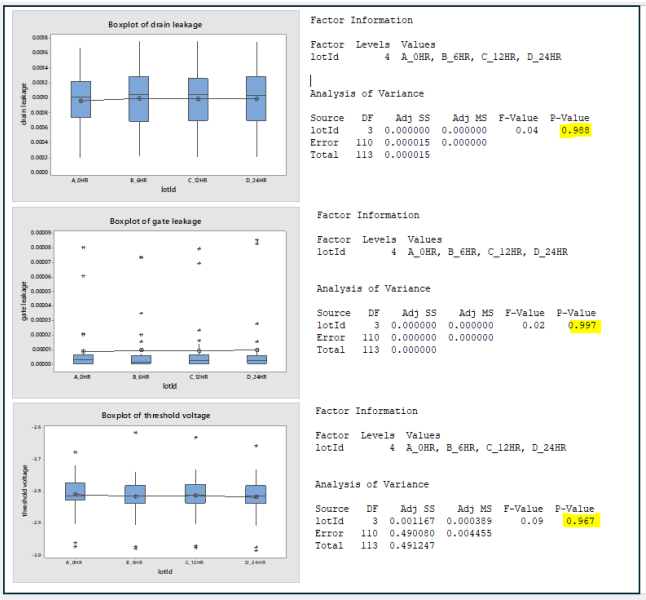

Fig. 5. One way ANOVA (Box plot representation) for ACP GaN on different waiting time intervals for retest.

The reduced retest waiting time study was conducted only at ambient temperature, as the objective was to avoid

introducing additional processing steps such as high-temperature testing.

5.0 CONCLUSION

With the 6-hour retest strategy, a 75% reduction in retest hold time would significantly enhance the test floor capacity and improve the cycle time for GaN products. With the reduction of the minimum waiting time from 24 to 6 hours prior to retesting GaN devices, the observed shifts due to trapping remain within acceptable limits and are unlikely to result in significant yield loss. This approach presents a more practical solution approach in production to cater to high volume demand.

6.0 RECOMMENDATIONS

Further evaluation of the 6-hour retest strategy at ambient temperature is recommended across other GaN technologies. Given that trapping behavior can vary by technology, additional conditions—such as higher temperature (>ambient temperature)can be explored for both Final Test and Wafer Test.

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