CHARACTERIZATION ON THE IMPACT OF DIRECT BONDED COPPER SUBSTRATE VOIDS ON THE THERMAL PERFORMANCE OF A POWER MODULE THROUGH COMPUTATIONAL FLUID DYNAMICS SIMULATION ANALYSIS

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ABSTRACT

This study investigates the impact of DBC voids at the copper–ceramic interface of Direct Bonded Copper (DBC) substrates on the thermal performance specially the thermal impedance of power modules, using Computational Fluid Dynamics (CFD) simulations. The DBC voids located beneath the semiconductor dice, where efficient heat dissipation is critical. Results of this study show that thermal impedance degrades by 20-30% depending on the location of the voids. These findings highlight the importance of minimizing voids—particularly beneath the die area—to maintain reliable heat transfer and structural integrity.

This study provides comparison of the effect of DBC voids to the heat dissipation of the device comparing to the baseline for defining substrate quality requirements and validate with the supplier specifications**.**

1.0 INTRODUCTION

Power modules are integral components in power electronics, responsible for efficiently managing the conversion and regulation of electrical energy. A critical aspect of the design is thermal management, as the performance and reliability of power modules depend heavily on effective heat dissipation.

Direct Bonded Copper (DBC) substrates are commonly used to hold the internal circuitry and isolate the active region from the heat sink in power modules due to the ceramic's excellent thermal conductivity and electrical isolation. Figure 1 illustrates a sample configuration of Silicon Carbide die mounted on a DBC substrate. The material structure of the DBC directly under the die is the path of heat dissipation.

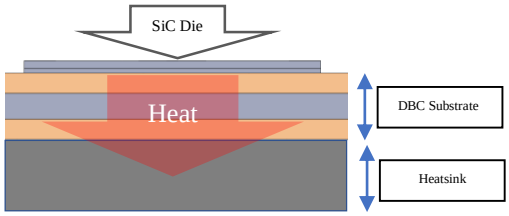


Figure 1: DBC Substrate Stack up with SiC Die

The presence of voids within the DBC material interface can significantly compromise the thermal performance, leading to increased thermal resistance, localized hotspots, and potential failure of the power module. DBC voids can form during the manufacturing process of the substrate due to imperfections in the material bonding, substrate handling, or thermal stress during processing. Upon power module assembly and end user application, these voids can disrupt the thermal path between the dice and the heat sink, impeding heat dissipation and causing high temperature gradients that may damage sensitive dice or components.

Understanding the impact of DBC voids on thermal performance is crucial for ensuring the life and reliability of power modules.

To evaluate the impact of voids in the power module DBC virtually, thermal simulation tool such as CFD was used in this study. Among all thermal simulation tool, CFD offers a powerful and efficient method for analyzing the thermal impedance of Direct Bonded Copper (DBC) in power modules. One key advantage

is its ability to provide detailed temperature distribution and heat flow insights across different layers of the DBC without physical prototyping. It allows users to model complex geometries, material interfaces (like copper–ceramic), and boundary conditions—such as heat sources, convection, and cooling strategies—with high accuracy. CFD also enables virtual testing of defects, such as voids or delamination, to understand their impact on thermal impedance. This helps identify thermal bottlenecks, optimize design, and improve reliability early in the development phase. Compared to experimental methods, CFD is faster, more flexible, and cost-effective, making it a valuable tool for evaluating and optimizing the thermal performance of DBC-based power modules.

2.0 REVIEW OF RELATED WORK

Refer to 1.0 Introduction

3.0 METHODOLOGY

The thermal characteristic of the power module with DBC voids under the die area were characterized in a 3D model with actual material property of the module parts. Using Computational Fluid Dynamics (CFD) simulations, four different void configurations were evaluated: (1) no voids as baseline, (2) voids on the top copper ceramic interface, (3) voids on the bottom copper ceramic interface, and (4) voids on both interfaces.

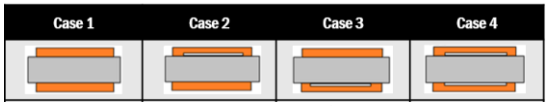


Figure 2. Side view illustration of the void locations

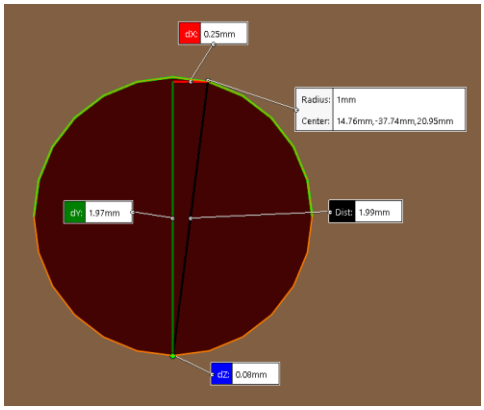


Figure 3. Void Size (D =2mm, 0.08mm height)

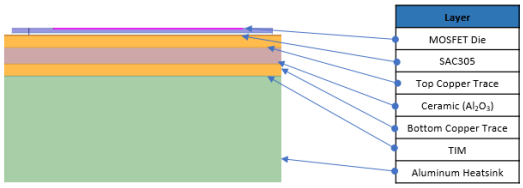


Figure 4. Side view illustration of the DBC layers with Al Heatsink

The boundary conditions used in this simulation, along with the extracted temperatures for each DBC layer, are outlined in Figure 4. A total heat generation of 85 W was applied to the active die volume (junction area). To control the temperature of the DBC case or bottom copper layer (Tc), as well as the die temperature (Tj), a fixed temperature of 60°C was applied to the bottom surface of the heatsink (Ts). Additionally, the ambient environment was set to an initial temperature of 60°C to match the device's starting temperature. The thermal simulation was run until the peak temperature was reached.

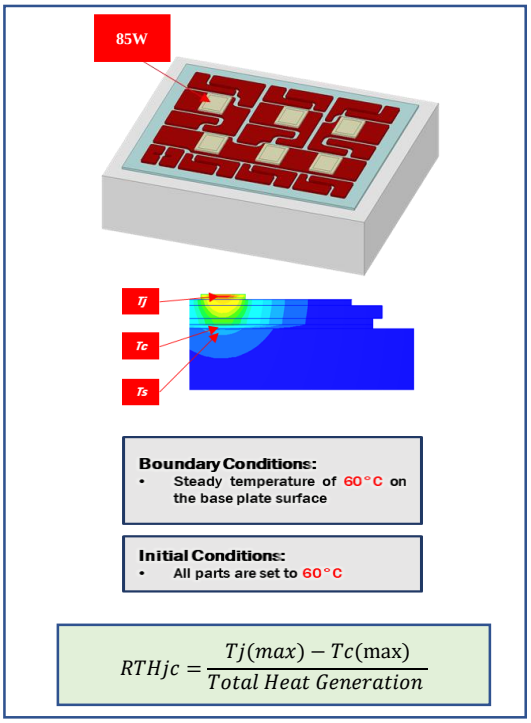


Figure 5. Boundary & Initial Conditions of the Simulation and Formula for Computation of the Thermal Impedance

After the simulation was done Tj, Tc and Ts has been extracted from the volumes and thermal impedance value was computed using formula in Figure 4.

4.0 RESULTS AND DISCUSSION

In this section, the results of the thermal evaluation of DBC substrates with different void configurations beneath the die area of a power module were presented and discussed. Each configuration was assessed based on the resulting thermal resistance, temperature distribution, and the formation of hotspots within the die area.

4.1 No DBC Voids (Baseline Condition/Control)

The computed thermal resistance is 0.678 C/W in this condition, and the heat dissipation occurred efficiently from the die to the substrate. The temperature rise was gradual and evenly spread, with a slight increase near the die due to the inherent thermal load. This scenario represents the ideal case where the DBC structure is fully intact, and the heat transfer path is uninterrupted by DBC void absence. The maximum temperature 158ºC with case temperature of 99.8 ºC under the area of the die was observed to be well within safe operating limits, indicating the effectiveness of the thermal management system under this condition. Very small hotspot area can be seen on top of the active die with uniform distribution.

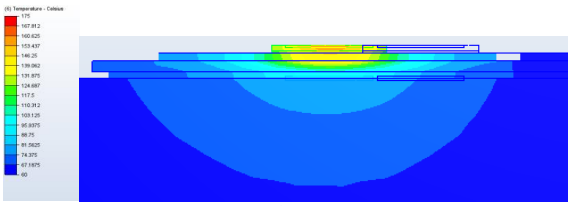


Figure 6. No DBC Voids Configuration (Cross Sectional View)

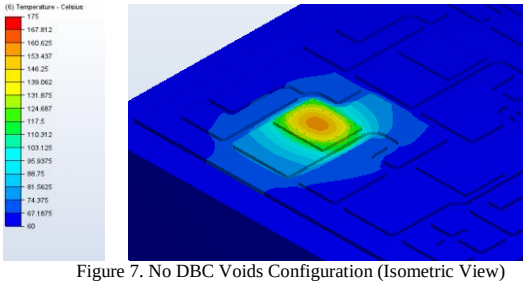


Figure 7. No DBC Voids Configuration (Isometric View)

4.2 Void in the Top Copper Interface with Ceramic

When void was introduced only in the top copper interface with the ceramic, the junction temperature increased significantly up to 165.9ºC with case temperature of 96.2 ºC directly under the die with DBC void. The void in the top copper created localized disruptions in the heat conduction path, leading to a higher thermal resistance of 0.819 ºC/Watt between the die and the ceramic substrate. As a result, the temperature response became worse, with noticeable hotspots forming in the areas above the die. The maximum temperature rise in the die area was approximately 8°C higher than the baseline condition. These hotspots were primarily located near the DBC void regions in the top copper interface, where the heat had to diffuse around the voids, reducing the overall heat dissipation efficiency. The increase in thermal resistance in this configuration to was attributed to the interruption of the heat conduction path from the die to the ceramic substrate, which would negatively impact the thermal stability and reliability of the power module.

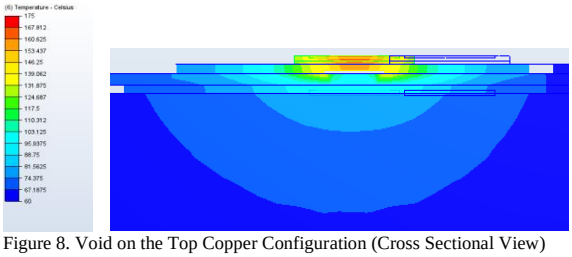


Figure 8. Void on the Top Copper Configuration (Cross Sectional View)

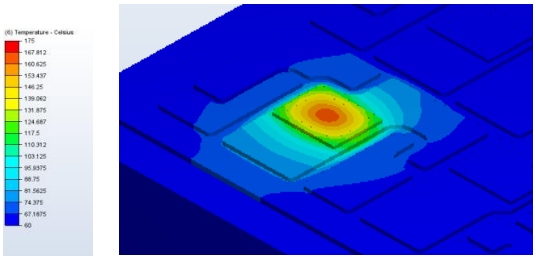


Figure 9. Void on the Top Copper Configuration (Isometric View)

4.3 Void in the Bottom Copper Interface with Ceramic

Introducing void only in the bottom copper interface with the ceramic, located under the die, led to a different thermal behavior. In this case, the heat transfer had a significant impact in the thermal behavior of the module, as the bottom copper layer serves as the primary heat conduit from the die to the substrate (RTH jc =0.906 C/W). Void in this region resulted in an increase in thermal resistance of around 34% compared to the baseline. The heat transfer from the die to the substrate was hindered, leading to a more pronounced temperature rise up in the die which resulted to a maximum temperature of 171ºC with case temperature directly under the die of 94.10ºC. Hotspots formed in the regions where the voids were present, particularly near the interface between the bottom copper and the ceramic substrate.

These hotspots were more concentrated than those observed in the top copper void scenario, as the void

in the bottom copper directly interrupted the thermal path beneath the die. This configuration demonstrated that void in the bottom copper had a more severe impact on thermal performance than void in the top copper.

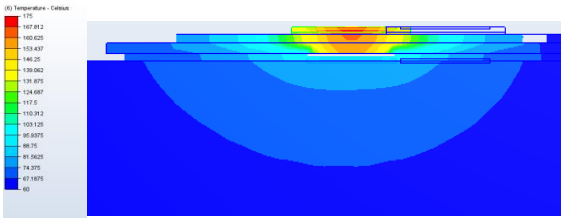


Figure 10. Void on the Bottom Copper Configuration (Cross Sectional View)

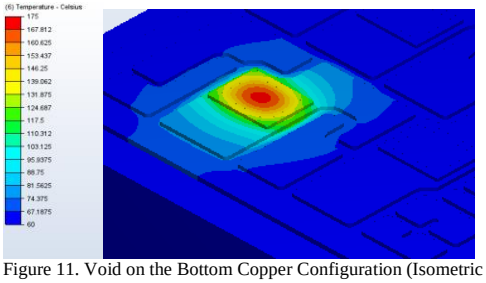


Figure 11. Void on the Bottom Copper Configuration (Isometric View)

4.3 Voids in Both Top and Bottom Copper Interface

The scenario with voids in both the top and bottom copper layers resulted in the highest thermal resistance (0.940 C/W) and the most significant temperature rise of the active die area to about 173.86°C with case temperature of 93.96 °C. The combined effect of voids in both copper layers created substantial barriers to heat transfer in both directions, significantly impairing the thermal management system.

The temperature distribution showed pronounced hotspots not only in the die area but also in the regions adjacent to the voids in both copper layers. The maximum temperature of the die increased by about 16.3°C compared to the baseline, and the thermal resistance was much higher (38% from the baseline) than in any other configuration. These findings highlight the compounded effect of DBC voids in both the top and bottom copper layers, where the thermal path was disrupted in multiple locations. The combined voids amplified the thermal inefficiencies, leading to potential reliability concerns in power modules, as the die would be exposed to high thermal stresses which can lower down the life of the module.

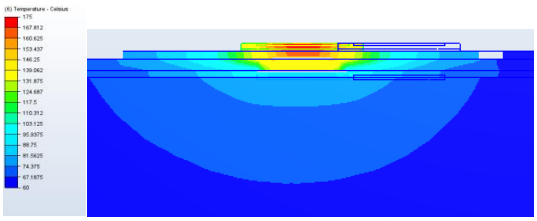


Figure 12. Voids on the Top & Bottom Copper Configuration (Cross Sectional View)

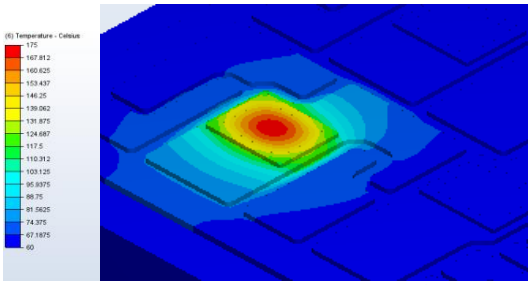


Figure 13. Voids on the Top & Bottom Copper Configuration (Isometric View)

4.4 Summary of Thermal Performance

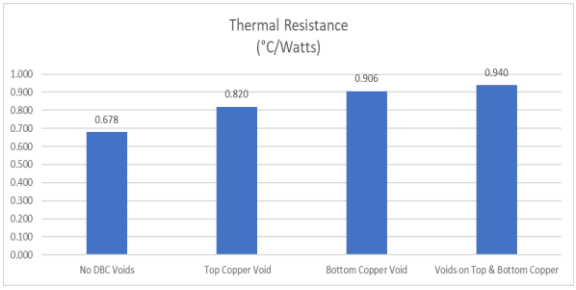


Figure 14. Thermal Resistance Comparison of the 4 Void Locations

As observed, the device with no DBC voids has a uniform thermal distributed in the DBC cross sectional area and got the lowest RTH value of 0.678 C/Watt. The presence of the voids on the top copper slightly increased the RTH to 0.820 C/Watt. While the presence of void on the bottom copper has a worsen the RTH value to 0.906 C/W which is almost have the same value with the presence of voids on Top and Bottom Copper of 0.940 C/W.

4.5 Implications for Power Module Design

The results from these simulations demonstrate the critical influence of DBC void location on the thermal management and performance of power modules. Voids in either the top or bottom copper interface negatively affect heat dissipation from the semiconductor die, with the bottom copper layer having a more pronounced impact. Specifically, a void in the top copper interface leads to an 11.79% increase

in thermal resistance, while a void in the bottom copper interface causes a more significant 31.32% increase. When voids are present in both copper interfaces, the thermal resistance rises by 33.66%, compounding the issue and resulting in substantial temperature increases. These findings highlight how the presence and location of voids can significantly degrade thermal performance and reliability, emphasizing the importance of minimizing voids—especially in critical areas beneath the die.

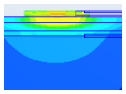
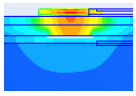
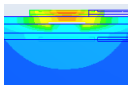
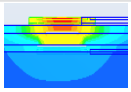
No Voids		Void in the Bottom Cu	
Void in the Top Cu		Void on both Top & Bottom Cu	

Table 1. Heat up beneath the die area of the DBC with and without voids

Visually, it can be seen that heating up in the area beneath the die having no voids is dissipating to the heatsink which lower down the temperature of the die and creates equal heat spreading in the cross section. While the heat in DBC with void in the top copper is trapped in the top cu and cannot dissipate in the heatsink causing the die temperature rise. While the heating up on the DBC with voids in the bottom copper of the substrate trapped the heat before it dissipates in the heatsink which causes worse thermal effect in the die. And among all the void location the void present in both top and bottom copper layer shows the worst heat spreading with heat trapped on top and bottom copper which results to worse thermal resistance among all configurations.

5.0 Conclusion

The thermal analysis of DBC substrates with different DBC void configurations under the die area of a power module reveals that DBC voids on the top copper interface, bottom copper interface, or both can significantly impact the heat transfer and lead to higher thermal resistance and localized hotspots. DBC voids on the bottom copper interface had the more severe impact than the top, while DBC voids on both interfaces compounded the thermal inefficiencies. These findings highlight the importance of being strict on the quality criteria of DBC voids on raw material suppliers in consideration of power module design & development to ensure reliable thermal performance and prevent potential failures due to thermal overload.

6.0 Recommendations

This study shows that voids in the DBC layer can significantly increase the thermal resistance of power modules, which can lead to overheating and reduced performance. To manage this risk, engineers should use detailed CFD simulations early in the design process to study how different void sizes and locations affect thermal resistance. And also determine what is the allowable and acceptable DBC void size that will not compromise the quality of the device.

To make this process faster and more efficient, AI and machine learning can be used to support thermal simulations. AI models trained on simulation data can quickly predict how voids impact thermal resistance, saving time and reducing the need for repeated simulations. These tools can also detect complex void patterns that may cause higher thermal risk.

By combining CFD with AI, design teams can help develop more design iterations & improve the accuracy of thermal analysis, speed up development, and build more reliable power modules that are better able to handle real-world manufacturing variations.

7.0 Acknowledgment

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To everyone mentioned, contributions have made a significant impact in the success of this study. The authors are honored to have had the opportunity to work with such talented and dedicated team. Looking forward to continued collaboration and shared achievement in the future.

8.0 REFERENCES

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