WAFER-LEVEL PACKAGE DEVELOPMENT OF FLIP-CHIP INTERCONNECTS FOR ULTRA-LOW RESISTANCE APPLICATION

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ABSTRACT

Understanding contact resistance is an important factor for flipchip (FC) devices, where interconnect performance is key to enable high efficiency and reliable devices for high power applications. Typical FC bumps with polyimide layer, copper post, and solder cap layering have contact resistance of 10mOhm, which may be high for low resistance applications. Plasma clean steps were explored by applying incoming plasma prior bump applications which lowered R_c to 3.9 mOhm, but robustness test by applying actual manufacturing scenario shows that this solution is not repeatable with wait-time-windows and plasma parameter variation. Application of aggressive plasma after PI process showed an even higher R_c of 52mOhm, suggesting degradation of contact pads. This led to a re-design of bump stack where PI layer was deposited first to remove contact of PI to Al pads, which gave a R_c of 0.7mOhm suggesting a new and novel bump solution to enable low resistance FC interconnects.

1. 0 INTRODUCTION

Continuous scaling of integrated circuits has pushed the industry to develop smaller, faster, and more powerful electronic devices that will address the need for high-performance and high-density solutions. One major interconnect solution that is being utilized to address this need is flip chip bonding, as it has better signal integrity, reduced thermal impedance, and improved contact area. As a result, FC devices are seeing a year-on-year growth of 7.30% in the next ten years, with expected technology market of around USD 45.22B by the year 2032 [1].

Flip chip (FC) bonding enables higher I/O density, smaller device footprint, and better electrical performance. Controlled collapse chip connection (C4) which uses solder bumps with larger dimensions are typically used for larger bump pitch >200µm. However, to better utilize die footprint, C2 micro-bumps, typically consist of micro copper pillars (CuP) with solder caps, are used to enable pitch <200µm [2]. CuP bumps can be direct on aluminum bump or bump on vias, either having a passivation stress buffer material like polyimide or ceramic layers like SiN or SiO_xN_y. Different variations of FC interconnects from C4 to smaller and smaller C2 bumps can be seen in Figure *1*.

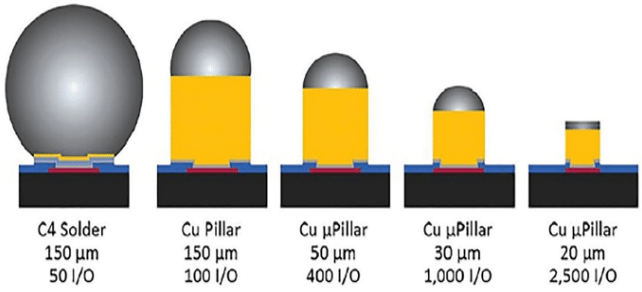

Figure 1: Different types of flip chip bump [2]

Compared to standard wire bond packages, FC packages enables lower resistance since die is directly connected to the substrate via CuP which is significantly shorter than wireloop. Typical CuP bumps have significant resistivity advantage (2-3 µΩ-cm) than aluminum interconnects (3-4 µΩ-cm). However, for power applications, low resistance interconnects play a big factor to improve performance that may degrade due to switching or thermal loss. In CuP structure solder joints contributes a big factor in conductivity loses as intermetallic compound (IMC) formed like Cu_6Sn_5 have resistivity of 17.5 µΩ-cm. Traditional solder bumps have been extensively employed for flip chip bonding due to their low cost, high electrical conductivity, and ease of processing. Nonetheless, their usage has several drawbacks. Solder joints are prone to various forms of corrosion, exhibit relatively higher contact resistance, and often experience significant migration during thermal stress tests.

To improve the IMC composition and thickness, Sn-Ag-Cu solder can be used instead of simply Sn-Ag solder. Cu in the solder can effectively decrease the Cu_5Sn_6 formation and improve the electromigration performance of solder joints [3].

Another possible cause of R_c increase is with contamination or unwanted material that may be present between the layer stack-up. This may be caused by an inherent material on the aluminum pad prior any bump process is being done like oxidation or fab induced contamination. Another root cause

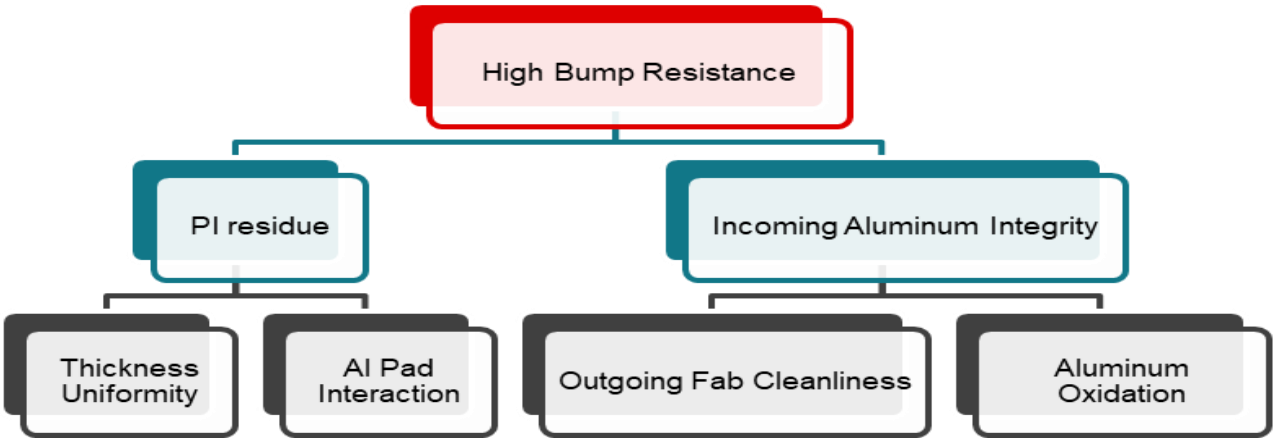

Figure 2: High R_c Fault Tree Analysis

might be thin film residue that is bump process induced like polyimide thickness variation or residue not being fully removed during plasma clean process. **Error! Reference source not found.** shows the fault tree analysis and various factors which may contribute to resistance increase.

These contributing factors increases up R_c to almost 10mOhm, which degrades device performance specially for high switching and high-power applications where efficiency is important. In this study, these factors are addressed in order to lower down R_c and improve product performance.

2. 0 REVIEW OF RELATED WORK

Refer to 1.0 Introduction.

3.0 METHODOLOGY

In this paper, plasma clean parameters and design stack-up was investigated for their effect in the bump contact resistance, R_c.

3.1. Impact of Plasma Clean Step

For the first split, S1, plasma clean, was added during incoming wafer before any layer was added to clean the aluminum contact pads from any possible thin film contamination.

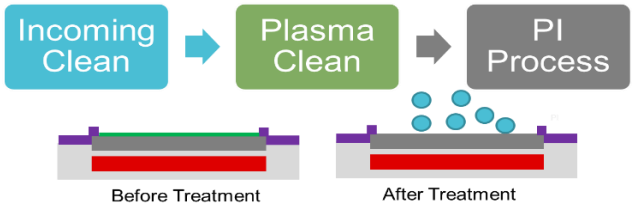

Figure 3: plasma clean step for incoming wafer clean

For split 2, S2, a more aggressive plasma process was implemented after polyimide layer deposition. This is to remove any material that might be still present on the aluminum bond pad.

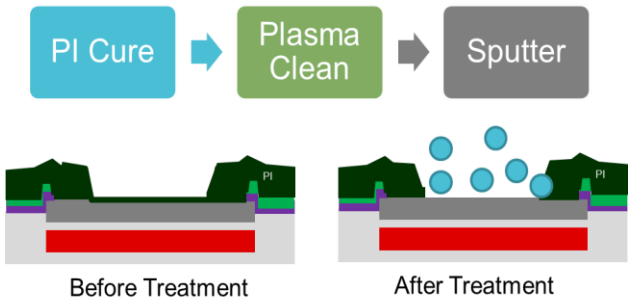

Figure 4: Aggressive Ash process after PI process

3.2. Impact of stack-up design

The layer stack-up of the CuP bump was changed to check for the impact in R_c. Split 3, S3, follows a CuP deposition first, followed by polyimide layer deposition. This stack ensures that there is no contact between the polyimide and the aluminum pad which can cause an increase in the resistance. Additionally, since R_c is inversely proportional to the cross-sectional area, A, an increase in A can effectively decrease R_c.

$$R_c = \frac{\rho L}{A}$$

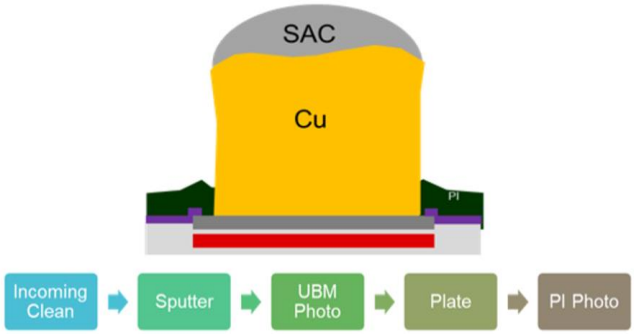

Figure 5: Process flow for CuP with polyimide-last

Each splits were then bumped on a test wafer with aluminum metal interconnects, and where tested for R_c.

4.0 RESULTS AND DISCUSSION

4.1. Plasma Clean Step

Plasma clean step was added during incoming processes to remove any native contaminants that might be present in the wafer during fab processes or transport induced. This may be any organic or inorganic contaminants, which upon adding bump layers, can be trapped between and cause an increase in R_c. For the plasma step, typical gas that is being used is O_2 which is reactive to organic substances. O_2 gas generated during ionic excitation from the plasma source reacts easily with any organic molecule that is on the surface. This converts long molecular chain of organic C-O-H into CO_2 and H_2O that can be vacuumed out from the chamber [4].

$$[R - O - H] + O^+ \rightarrow CO_2 + H_2O$$

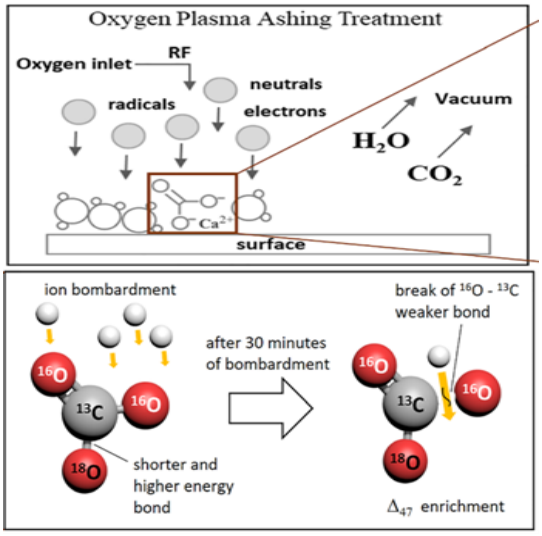

Figure 6: Schematic diagram for O2-ash reaction[4]

Probing the wafer for S1 shows a decrease in contact resistance reaching 3.9 mOhm. This suggest that plasma clean process was successful in removing possible contamination prior any bump layers was added.

However, the data collected was processed in a highly controlled scenario with no queuing between process steps in Figure 3. To test the manufacturability of this split, wait-time window (WTW) was imposed to simulate real manufacturing conditions where material does not easily load from a single process step to another. WTW 1 was process between incoming clean and plasma clean, while WTW 2 was process between plasma clean and PI coating step. A WTW of 24 hours and 72 hours was imposed for both WTW step to simulate even extreme ageing conditions. Additionally, power, pressure, and gas flow were also varied to simulate process variability within the machine itself.

Table 1: Manufacturability DOE for incoming ash process, S1

WTW1	WTW2	Gas Flow	Pressure	Power	R_c, [mOhm]
24	24	High	Low	High	17
24	24	Low	High	High	3.7
24	24	Low	Low	Low	8
24	24	High	High	Low	11
24	72	High	High	Low	26
24	72	High	Low	Low	37
24	72	Low	High	Low	19
24	72	Low	High	High	28
24	72	High	High	High	23
72	24	Low	Low	Low	22
72	24	High	Low	Low	14
72	24	Low	Low	High	34
72	24	Low	High	Low	33
72	24	High	High	High	30
72	24	High	High	Low	24
72	72	Low	Low	Low	34
72	72	High	High	Low	16
72	72	High	Low	High	17
72	72	Low	High	High	30

After doing the DOE, only a single split passed, suggesting that an incoming plasma clean solution is only good for a controlled scenario and is not repeatable and manufacturable by accounting actual line conditions.

For S2, a more aggressive plasma process was imposed. The idea is similar to the schematic shown in Figure 6, but the higher power of the plasma ions should be able to remove any PI residue that might be left post PI process. This was done since after analyzing the initial condition of the PI opening without any of the treatment done via time-of-flight secondary ion mass spectrometry, an increase in the carbon concentration can be found localized along the PI opening, suggesting organic contamination present causing increase in

R_C as shown in Figure 7. This residue, even with plasma process involved, was attributed to a possible reaction between the inherent native oxide film of aluminum and polyimide causing the formation of unwanted organometallic composite film [5], [6].

However, upon doing contact resistance check for S2, which has a more aggressive plasma process, an even higher R_c was acquired of 52mOhm. This can be attributed now to an increase in the effective etch rate which damages the aluminum pads causing areas for potential material redeposition which increases R_c.

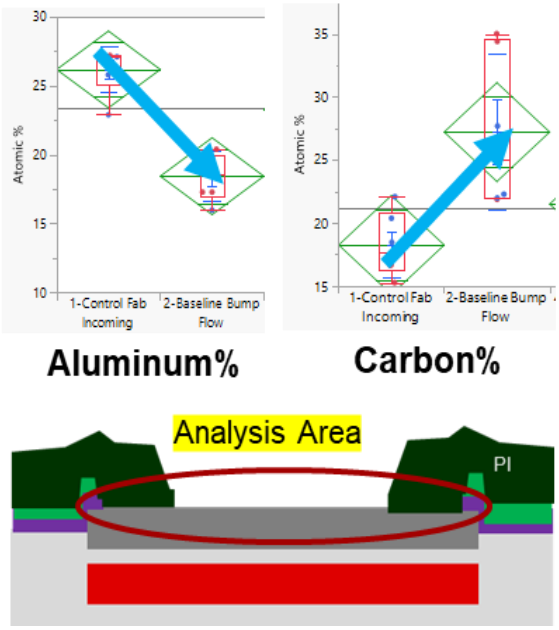

Figure 7: TOF-SIMS analysis of PI opening post PI process

4.2. Impact of Stack Design

Since PI thin film reaction with native oxide can be seen as a potential cause of increase in R_c, S3 was devised so as to isolate any contact of the aluminum pads to PI layer. This was done by depositing first the copper post layer, followed by PI process. Depending on the initial PI opening, this solution also theoretically reduces R_c by a factor given by the equation below:

$$\Delta R_c\% = \left[1 - \frac{d_i^2}{d_{Cu}^2}\right] \times 100$$

where d_i is the PI opening and d_{Cu} is the copper post diameter.

After probing S3, a contact resistance of 0.7mOhm was acquired which is ultra-low resistance which can be used for high power, high switching applications necessary to meet requirements in improving efficiency of TI's devices.

To check as well if this solution is manufacturable, similar to Table 1, a manufacturability DOE was also done to simulate the effect of WTW before incoming process and seed deposition process. The DOE was done for the pre-sputter etch process, since this was the first plasma cleaning step after incoming clean processes. WTW of 24 and 72 hours was analyzed, as well as power and gas flow to simulate again the manufacturing variations.

Table 2: Manufacturability DOE for a polyimide-last re-design

WTW	Power	Gas Flow	R_c [mOhm]
24	Low	Low	1.85
24	Low	High	1.45
24	High	Low	1.55
24	High	High	1.2
72	Low	Low	0.25
72	Low	High	1.25
72	High	Low	1.25
72	High	High	0.94

After wafer probing of the DOE, it was observed that all the splits passed suggesting the robustness of re-design solution in meeting an ultra-low bump contact resistance for CuP FC interconnect.

5.0 CONCLUSION

By analyzing the various factors contributing to the increase in contact resistance, it was deduced that possible PI film residue contributes greatly to the increase in R_c. Different plasma cleaning steps were made to improve this, but PI-Al interaction was found to be very strong to be easily removed which makes plasma process not a viable solution.

A redesign of the bump structure, where the CuP was deposited first proved to be a solution of choice, where R_c was seen to decrease from 10mOhm down to 0.7mOhm. This solution should enable growth in high power and high switching devices requiring low resistance applications for improved efficiency and reliability.

6.0 RECOMMENDATIONS

Even though a bump stack re-design solution shows the lowest R_c, it is still worth exploring other possible solutions that can lower R_c for especially different plasma sources and gases that may be able to lower down further R_c.

7.0 ACKNOWLEDGMENT

The authors would like to thank Texas Instruments Philippines Inc. for supporting this study which is beneficial

to understand resistance increase in CuP interconnects. Special acknowledgements to Dr. Jungwoo Joh from TI's Advance Technology Development group for supporting the wafer probe resistance measurement, to Dr. Al Griffin of TI's Quality Team for his help in doing TOF-SIMS and advance characterization, and to the Clark Bump Manufacturing Department for helping in processing the splits and wafers for this study.

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