

ELIMINATION OF WIRE SHORTING DEFECT ON MEMS DEVICE THROUGH WIRE ANGLE DESIGN OPTIMIZATION

Frederick Ray I. Gomez

Freddie B. Folio

Anthony R. Moreno

New Product Introduction

STMicroelectronics, Inc., 9 Mountain Drive, LISP II, Brgy. La Mesa, Calamba City, Laguna 4027

frederick-ray.gomez@st.com, freddie.folio@st.com, anthony.moreno@st.com

ABSTRACT

Microelectromechanical systems (MEMS) package is the assurance of improvement for consumer and industrial applications and performances with lower power consumption and less invasive than other larger devices. The paper incorporates new MEMS device with a multi-stacked dice configuration, with assembly challenges encountered at wirebond process. MEMS complex stackup and die size variation packed in a single dimension package to cope with the current die technology advances pose these challenges. With the package miniaturization trend and development, the wirebond machine capabilities were challenged. Parameters such as loop direction, speed, machine to machine variation are the factors contributing to risks of failure during the process.

Wire to die shorting was the top wirebond process defect contributor in terms of defect parts per million (PPM) of the MEMS MY24 Argentera device, with 718 PPM. To address the issue, series of technical discussions, package simulations and critical process validations were done. Tools such as the Theory of Inventive Problem Solving (TRIZ) tools, Ideal Final Result (IFR), Kano model, and S-curve analysis were used as a guide to analyze and assess the problem and help produce the right solution. Succeeding technical discussions revealed that the wire shorting defect is still occurring at 46 degrees steepest wire angle based on engineering data. Therefore, it is necessary to further analyze and optimize the current design with respect to the wire angle and clearances. This time, the Monte Carlo Simulation Method is used to check the PPM response given the existing wire angle, clearances, and tolerances. A new recommended die placement reference was generated, considering the results of the Monte Carlo Simulation and inputs from technical discussions. Ultimately, the wire angle parameter for top die to bond finger wirebonding was established and formulated from non-existing to 48 degrees steepest wire angle in absolute value with 90 degrees maximum, and applicable to die stackup of up to 235 μm .

A Design of Experiments (DOE) evaluation plan was formulated for corner lot validation, focusing on five legs with different die placements to understand the criticality of the observed wirebond issue. The corner validation for wirebond process successfully eliminated the wire-to-wire and wire-to-die shorting defects, with process capability of key output parameters measured for die shear test (DST), ball shear test (BST), wire pull test (WPT), and stitch pull test (SPT). Package modeling and simulation was done to verify the effect of the adjusted die placement to achieve the optimized 48 degrees wire angle in terms of the parasitic Resistance, Inductance, and Capacitance, and resulted to no significant difference in terms of these parameters between the previous layout and the adjusted die placement. Reliability tests were also done on the device and it passed all package and electrical oriented tests, mechanical stress tests, and environmental stress tests. With all the validations and tests passed, the new wire angle parameter for top die to bond finger wirebonding of 48 degrees was successfully evaluated, with 0 PPM achieved on the wire shorting occurrence. Moreover, the wire angle value was then recommended to be incorporated in the design rules for MEMS products.

1.0 INTRODUCTION

MEMS devices are the top volume runners in the market because of the fast-paced innovation in the digital world, such as phones and tablets. However, with continuous technological trends, breakthroughs, and state-of-the-art platforms, challenges in assembly manufacturing are inevitable. These challenges may arise from constraints in equipment, manufacturability, design aspects, or material compatibility

The first engineering builds of the MEMS MY24 Argentera device in focus experienced good results in terms of engineering yield. However, during the succeeding lots for the safe launch builds for pre-production, a critical issue arose in the wirebond process due to wire-to-wire and wire-to-die

shorting, as shown in Fig. 1. This issue could result in quality problems when the device moves into production.

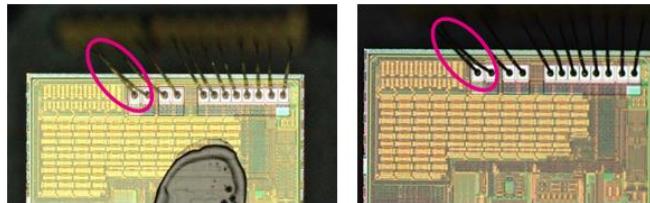


Fig. 1. Wire shorting defect on MEMS MY24 Argentera device.

Wire to die shorting was the top wirebond process defect contributor in terms of defect PPM with 718 PPM as shared in the chart in Fig. 2 during large-scale engineering build for safe launch prior pre-production. In anticipation, it would produce when it goes to mass production. The situation became a big challenge since the device already completed the engineering qualification builds and the next product maturity phase would mean that the parameters will be frozen. With this, it is critically important that the wirebonding issues be resolved immediately.

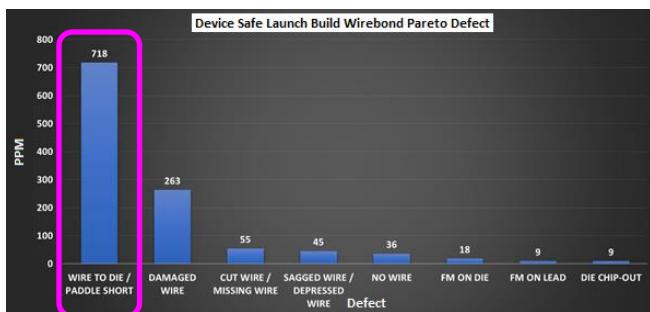


Fig. 2. Wirebond process defect PPM level chart.

The goal of the study, or the voice of the customer (VOC) is to mitigate the wire-to-wire and/or wire-to-die shorting defect on MEMS MY24 Argentera device. To address the issue, series of technical discussions, package simulations and critical process validations were done. The team conducted a corner lot validation that focused on five (5) legs with different die placement to understand how critical the observed wirebond issue is. The optimization of die placement and the wirebond process were focused on the wire angle of the steepest part and longest wire of the wirebond loop. Ultimately, the wire angle parameter for top die to bond finger wirebonding was established and formulated from non-existing to 48 degrees minimum, as highlighted in Fig. 3. The package design also ensured that the other design parameters are fulfilled. Note that the wire angle optimization applies only to the current die stackup height of up to 235 μm .

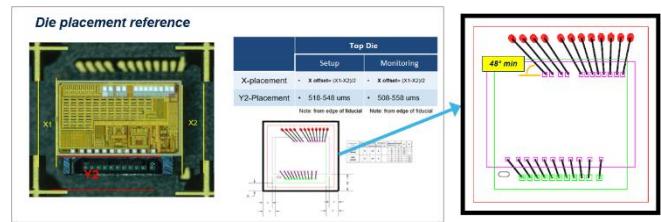


Fig. 3. Wire angle parameter formulation from die placement optimization.

2. 0 REVIEW OF RELATED WORK

The 5 legs were closely monitored at other critical processes at end-of-line (EOL) stations, especially during the mold process, laser marking, and package singulation, until the assembly was completed to observe the response per leg. Using the package stack-up calculator shows that no violations will cross the line, as shown in Fig. 4.

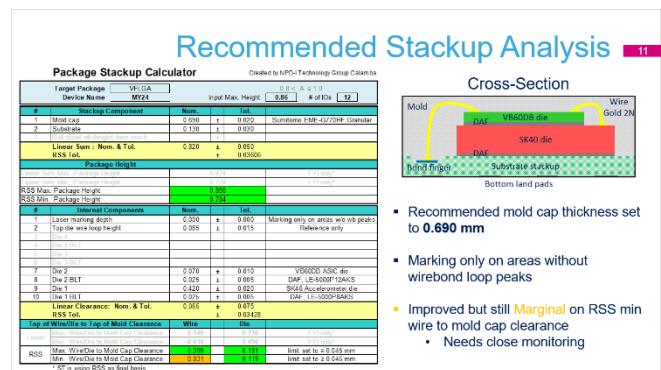


Fig. 4. Package stackup calculator.

The corner validation for wirebond process successfully mitigated the wire to wire and wire to die shorting defects, as shared in the PPM chart in Fig. 5.

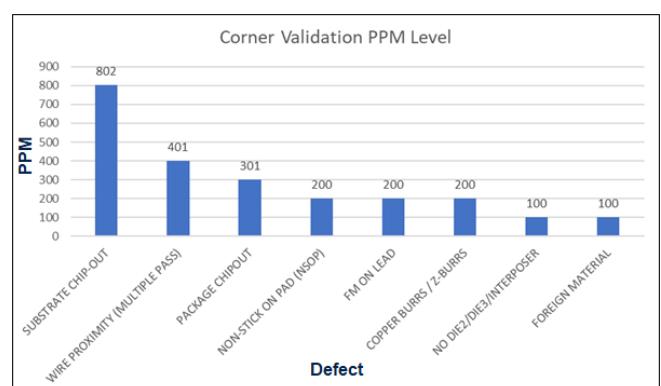


Fig. 5. Wirebond process defect PPM level chart, with no PPM for wire shorting defects.

3.0 METHODOLOGY

TRIZ tools were used as a guide to analyze and assess the problem and help produce the right solution. S-curve analysis was also used to help decide the right technique to apply, as shown in Fig. 6 and Fig. 7. Kano model in Fig. 8 was also used as guide to determine the VOC or goal and the critical to qualities (CTQ) that is to improve the wire shorting defect reduction, from 718 PPM to less than 100 PPM prior mass production.

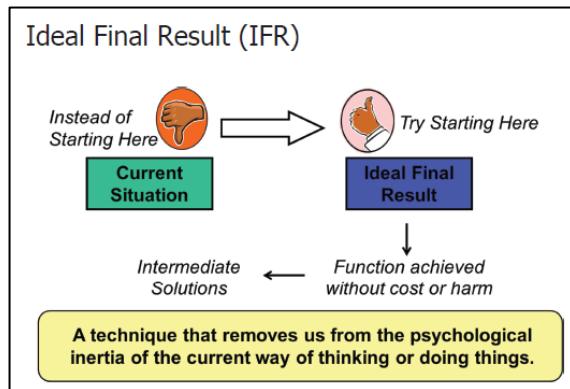


Fig. 6. IFR representation.

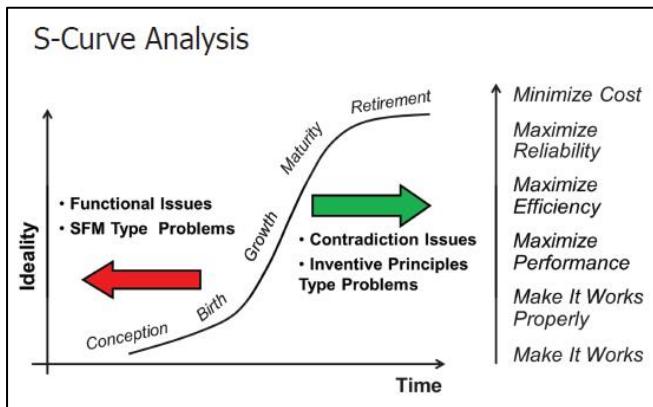


Fig. 7. S-curve analysis to help identify the suitable technique the problem.

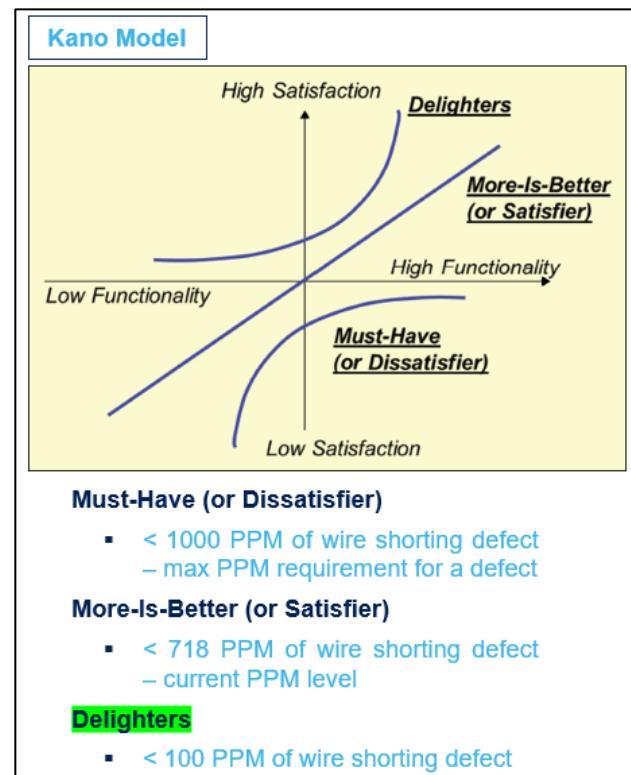


Fig. 8. Kano model showing the target PPM level.

Contradiction and principles are then used with the identified TRIZ and parameters that are features to improve and the “strength” of the bonded wires not to produce wire shorting defect and the “length” of the wires as the features to preserve. Systems evolve for TRIZ towards ideality by overcoming these contradictions

- Ease of Manufacture
- Reliability

Risk assessment was done based on the package design review and feasibility. Three items were identified as shown in Fig. 9.

Fig. 9. Risk assessment table.

Package feasibility and design review of a new device are part of the design FMEA, which focuses on the assembly design rules and package stack-up analysis. MEMS MY24 Argentera is a Class II device, meaning it has a technology and/or package baseline. For comparison, a Class I device is a new device without a baseline, hence an R&D activity, while a Class III device is a version of an existing device and has no change in terms of the technology or the package. Since the MEMS MY24 Argentera device is a Class II device, it can refer to existing Design Failure Modes and Effects Analysis (DFMEA) available from other MEMS devices.

One reference is given in Fig. 10 from a MEMS device with a more complicated configuration than that of the MY24 device.

Fig. 10. DFMEA of MEMS device.

Based on the DFMEA, the package feasibility, and risk assessment, the risk of wire shorting defect occurrence on the top of the die to bond fingers wire group was not mentioned or identified. The actual occurrence was only 1 out of approximately 4000 assembly units (equivalent to 85 PPM) during the engineering build. Nevertheless, the wire shorting defect occurrence was captured during the safe launch build with approximately 10,000 assembled units. Referring to the DFMEA as a guide, the default action was to perform process optimization focused on the wirebonding process. Quick actions were taken to address the issue by optimizing the wirebond machine parameters and replacing the wirebonding tooling. However, the wire shorting defect was still observed after implementing the discussed measures. Intermittent wire shorting defects were reported by the production personnel during visual inspection. Fig. 11 wire to wire issue.

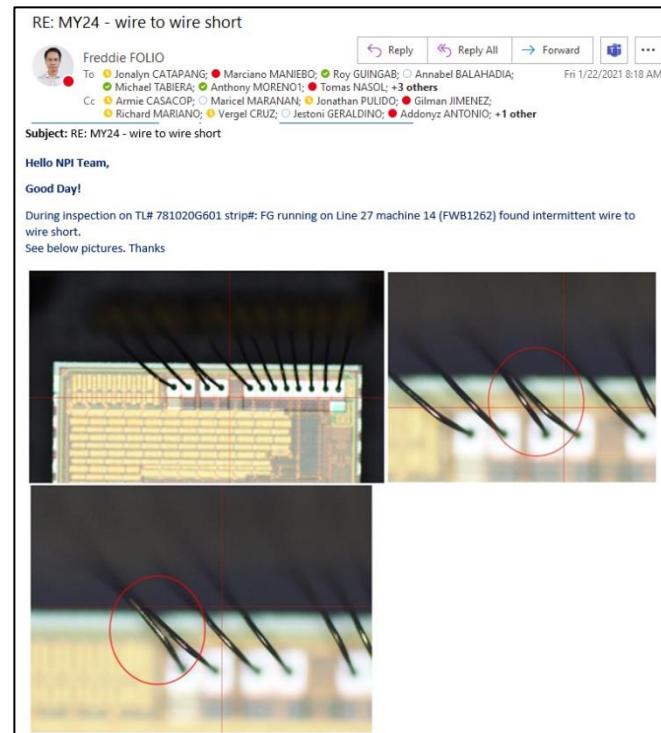


Fig. 11. Reoccurrence of wire shorting defect.

Further meetings and technical discussions were held, and the following items and recommendations were identified.

- Review internal design rule for MEMS if wire to die angled loop < 45 degrees can be adjusted to justify wire clamp gap tolerances
- Option to revisit die placement
- Simulation of existing wire angle
- Compare other MEMS devices

TRIZ was also done in Fig. 12 with the following identified parameters of contradiction:

- Improving features – Ease of manufacture, Reliability
- Worsening features – Length of stationary object, Strength

Fig. 12. TRIZ contradiction table

Among the TRIZ inventive principles identified in the matrix, principle #17 is the most applicable. Shown in Fig. 13 is TRIZ principle #17 with examples. The identified principle is aligned with the recommendations identified during technical discussions.

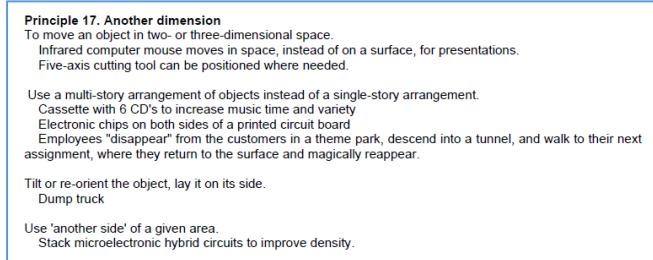


Fig. 13. TRIZ principle.

It is now imperative to revisit the MEMS design rules shown in Fig. 14. Upon checking the document DM00686274 1.0 MEMS Sensor Assembly Rules Manual Full Mold Packages, I noticed that it only has the die edge to bond pad edge angle specification (D1alpha) and does not yet include the wire angle between the top die and the bond fingers or leads.

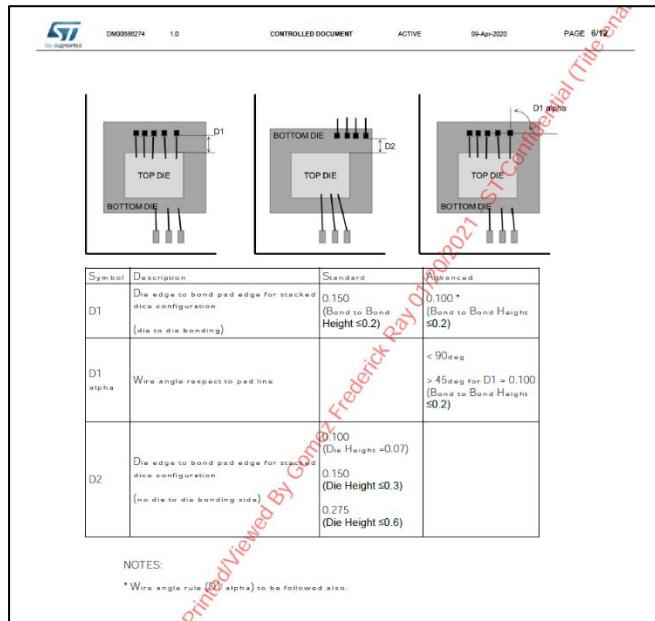


Fig. 14. Mems design rule showing the concerned clearances.

Fig. 15 shows the specification for the bond finger to die edge clearance (C6, C6A). Notice that no wire angle specification is defined. As mentioned earlier, only D1alpha is present in the specifications, and not yet for the supposed C6alpha or C6Aalpha. For the MEMS MY24 device, the affected wire and wire angle is the C6Aalpha.

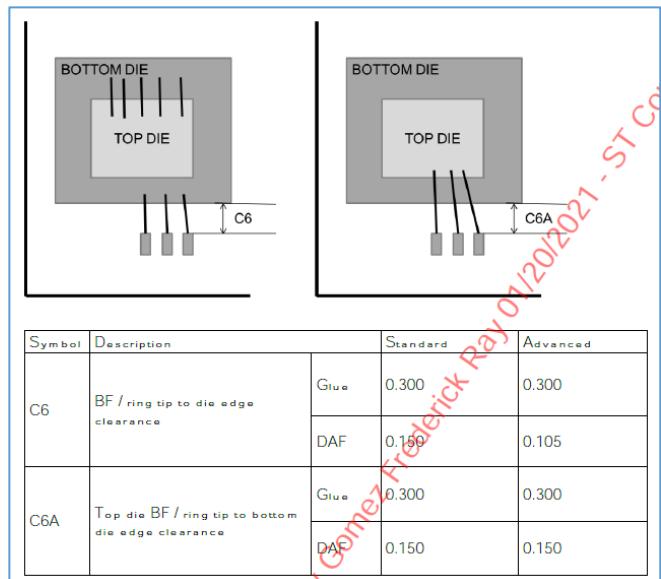


Fig. 15. Mems design rule on bond finger to die edge clearance.

Sharing the wide overview that comparing the wire angles for different MEMS devices in Fig 16 and the table of wire angle comparison in Table 1.

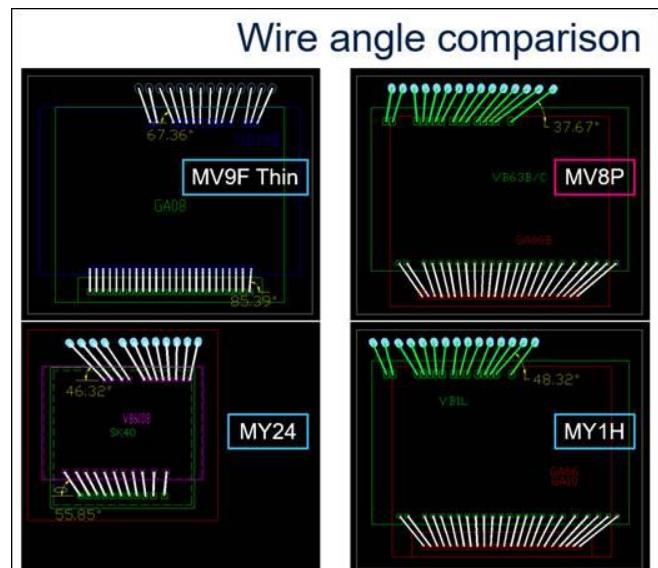


Fig. 16. Wire angle comparison of MEMS devices.

Table 1. Wire angle comparison of MEMS devices.

Device	Angle of steepest wire	Remarks
MY24 Argentera	46.32 deg	
MV9F Thin	67.36 deg	OK, standard WB

MV8P Suwon2.5	37.67 deg	Hybrid WB implemented (standard + RSOB)
MY1H SWAN2.7	48.32 deg	OK, standard WB
Specs	None	Need to define a new one

4.0 RESULTS AND DISCUSSION

Succeeding technical discussions revealed that the wire shorting defect is still occurring at a 46-degree wire angle based on engineering data. Therefore, it is necessary to further analyze the current design with respect to the wire angle and clearances. This time, the Monte Carlo simulation method is used to check the PPM response given the existing wire angle, clearances, and tolerances.

Many hand calculations were done to formulate the expression to be used in the Monte Carlo Analysis. Fig. 17 shows the current mount and bonding diagram (MBD) with the corresponding wire angle and clearances to be used in the formulation.

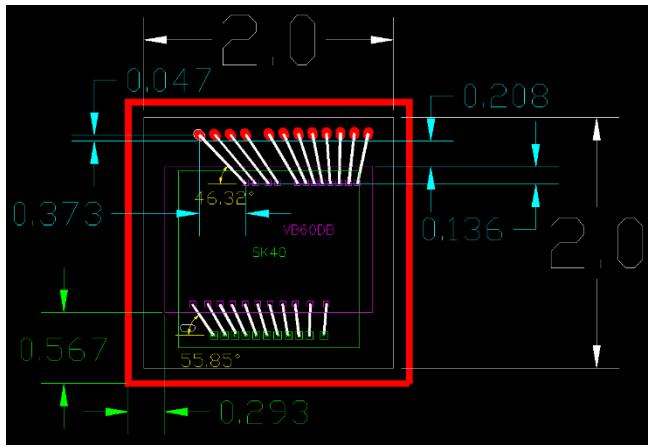


Fig. 17. Current MBD with measurement.

Wire end to tangent of bond finger (BF) = 0.047 mm

BF to die edge clearance = 0.208 mm

Die edge to wire end at bond pad = 0.136 mm

Total Y distance of wire end to end = $0.047 + 0.208 + 0.136 = 0.391$ mm

wire angle, C6Alpha = 46.32 deg

X distance of wire end to end = 0.373 mm (measured in CAD)

To verify the X distance using formula:

$$\tan(C6Alpha) = \tan 46.32^\circ = \frac{0.047 + 0.208 + 0.136}{X_{wire}}$$

$$X_{wire} = \frac{0.391}{\tan 46.32^\circ} = 0.373 \text{ mm}$$

Formula for the C6Alpha would be

$$C6Alpha = \tan^{-1} \frac{0.391}{0.373}$$

Expanding the formula of C6Alpha to include the variation of the clearances and die size.

$$C6Alpha = \tan^{-1} \left(\frac{0.047 + 0.208 + 0.136 + dsY + dpY}{0.373 + dsX + dpX} \right)$$

dsX, dsY = ASIC die size tolerance, X, Y, based on the kerf width or die blade thickness of 0.030 mm to 0.040 mm.

The ASIC die size uses the 0.035 mm kerf width. Assuming the nominal die size at 0.035 mm kerf width, then the tolerance at all 4 sides of the die would be $|0.040 - 0.035| / 2 = \pm 0.0025$ mm.

Hence, dsX and dsY normal distribution parameters would be

mean = 0 (when 0.035 kerf width is used)
standard deviation = $0.0025 / (3*1.67)$

dpX, dpY = die placement, X, Y, based on die attach machine capability of ± 0.025 mm X-Y tolerance.

Normal distribution parameters of dpX and dpY would be

mean = 0
standard deviation = $0.025 / (3*1.67)$

The equation for the wire angle and the parameters for the die size variation and die placement variation will then be used in Monte Carlo Analysis.

With the equation and the parameters derived previously, Monte Carlo simulation is done using the Minitab statistical tool as shared in Figs. 18-20. Sample size, N, is set to 10000, which is the required number of units during the safe launch build of the device.

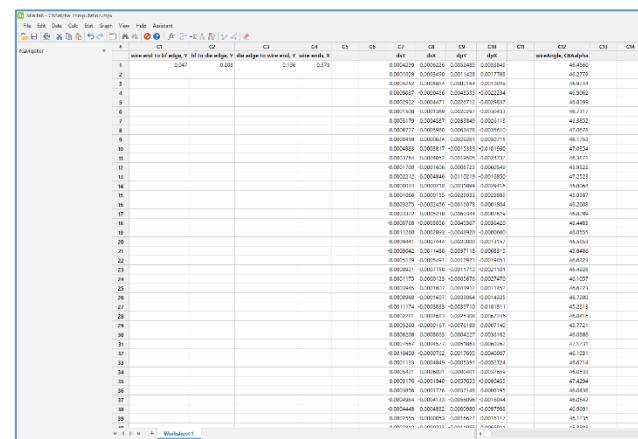


Fig. 18. Input data and output response, in Minitab.

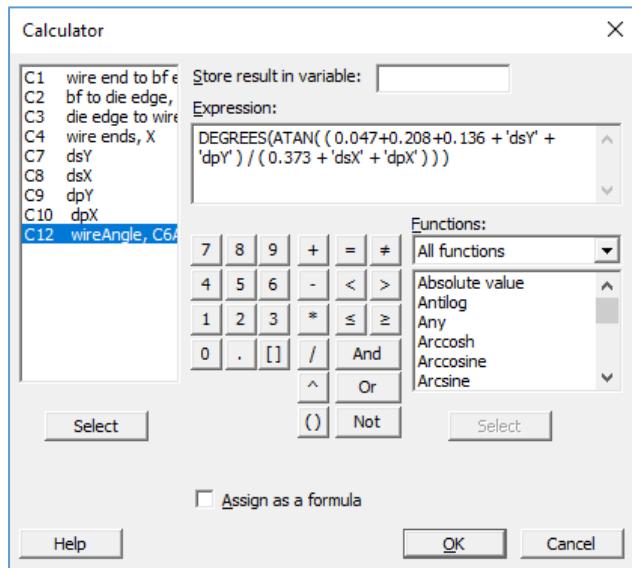


Fig. 19. Formula of the output response.

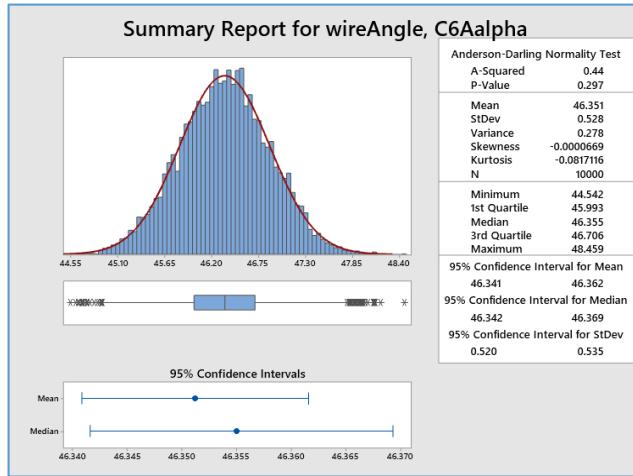


Fig. 20. Graphical summary, with P-value = 0.297.

Since P-value of 0.297 is greater than 0.05 (P-value > 0.05), hence, there is no significant difference in the wire angle distribution with that of a Normal distribution.

Alpha risk, $\alpha = 0.05$ (Confidence interval = 95%)

Capability analysis is done for Normal distribution to check the overall performance, and eventually define the value or limit wherein the PPM level would be at < 100 . Setting the USL to 48 deg, the corresponding PPM level is shown in Fig. 21.

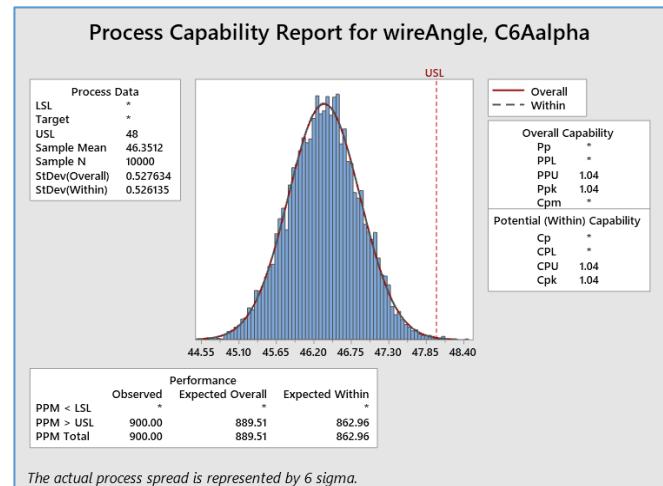


Fig. 21. Process capability report with USL = 48 deg.

PPM $>$ USL is at 900 observed and expected within at 862.96. Iteration of USL is done to eventually achieve the PPM level at < 100 . Fig. 22 shows the increments of USL conducted for process capability.

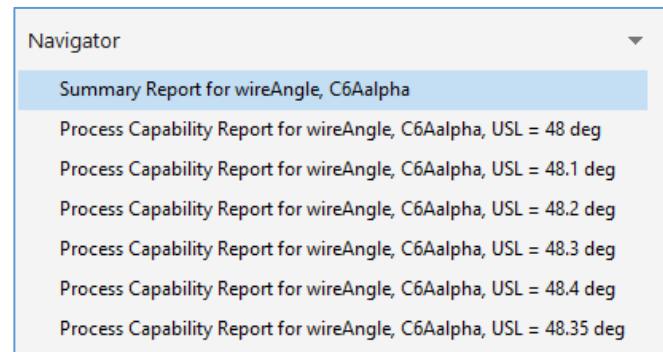


Fig. 22. Process capability report at different USL.

Finally, the target PPM level of < 100 PPM is achieved at USL set to 48.35 deg, as depicted in Fig. 23.

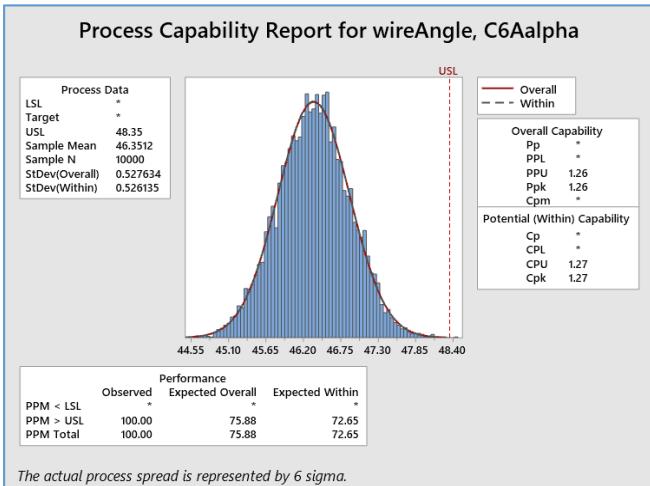


Fig. 23. Process capability report with USL = 48.35 deg.

PPM > USL is at 100 observed and expected within at 72.65. This satisfies the target of PPM level of less than 100, with the new C6Alpha value of 48.35 deg. The wire angle of MY24 device was then adjusted to 48.35 deg. Interestingly, the value is almost the same as the MY1H device with 48.32 deg that is already running in mass production.

A new recommended die placement reference was generated, considering the results of the Monte Carlo simulation and inputs from technical discussions. A Design of Experiments (DOE) evaluation plan in Fig. 24 was formulated for corner lot validation, focusing on five legs with different die placements to understand the criticality of the observed wirebond issue. Each DOE leg has been allotted 2,000 units, totaling 10,000 units for the corner lot validation with five legs. The optimization of die placement and the wirebond process focused on the wire angle of the steepest part and the longest wire of the wirebond loop. Linear analysis or the worst-case method was used to maximize the possible placement of the dies based on machine capability. The new MBD has a wire angle of 48.35 degrees as shown in Fig. 24.

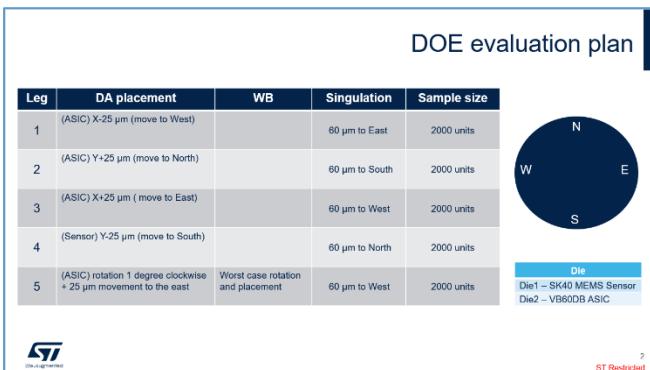


Fig. 24. DOE matrix.

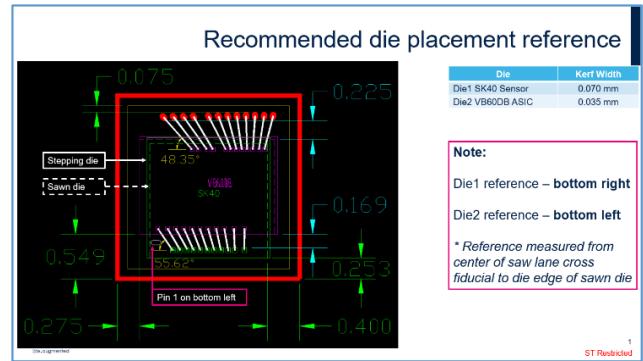


Fig. 25. New MBD and recommended die placement reference.

The 5 legs were closely monitored from other critical processes at end of line (EOL) stations especially at mold process, laser marking, and package singulation until the assembly completion to see the response per leg. The corner validation for wirebond process successfully mitigated the wire-to-wire and wire-to-die shorting defects, as depicted in the PPM chart in Fig. 26.

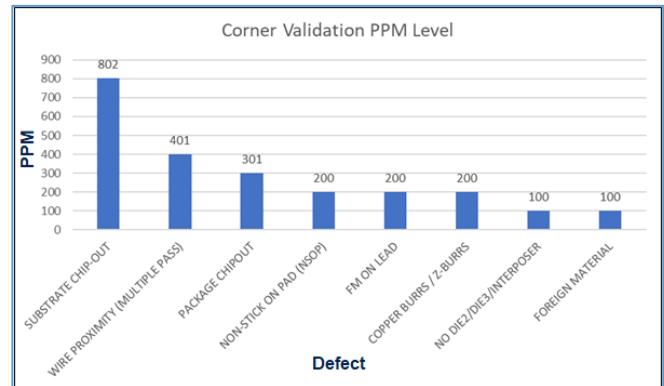


Fig. 26. Wirebond process defect PPM level chart, with no PPM for wire shorting defects.

The new wire angle parameter, C6Alpha, for top die to bond finger wirebonding of 48.35 deg was successfully evaluated, with PPM level of 0 achieved which satisfies the requirement of < 100 PPM. Moreover, C6Alpha is established and formulated from non-existing to 48.35 deg minimum. The value is then recommended to be incorporated in the design rules for MEMS products.

Process capability reports in Figs. 27-33 for the die shear test (DST), ball shear test (BST), wire pull test (WPT), and stitch pull test (SPT) during corner lot validation are shown in the corresponding charts. The results are provided for the DST of both Die1 Sensor and Die2 ASIC. For the wirebond output bond tests, namely BST, WPT, and SPT, the results are for the Die2 ASIC, which is the topmost die. A normality check was done, and all the data, except for the WPT of Die2, showed no significant difference in process variability

distribution compared to a normal distribution. Capability analysis for non-normal data was performed for the WPT of Die2, with the best-fitting distribution identified.

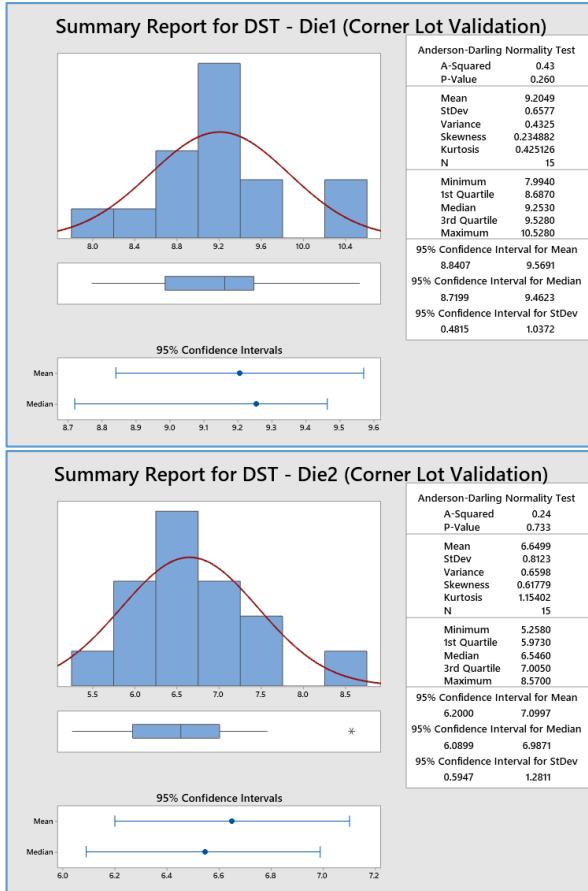


Fig. 27. Graphical summary of DST, with P-value = 0.260 and 0.733, respectively.

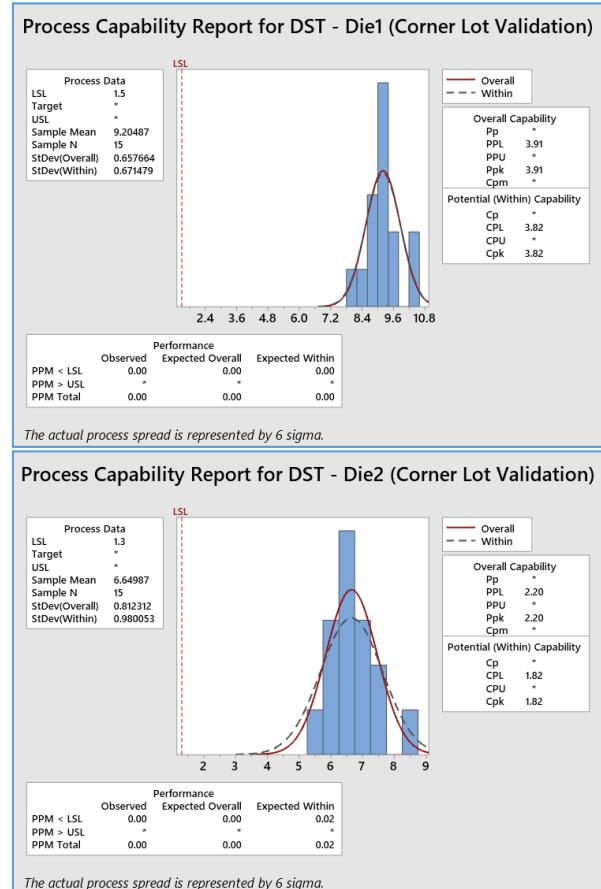


Fig. 28. Process capability of DST, with Ppk = 3.91 and 2.20, respectively.

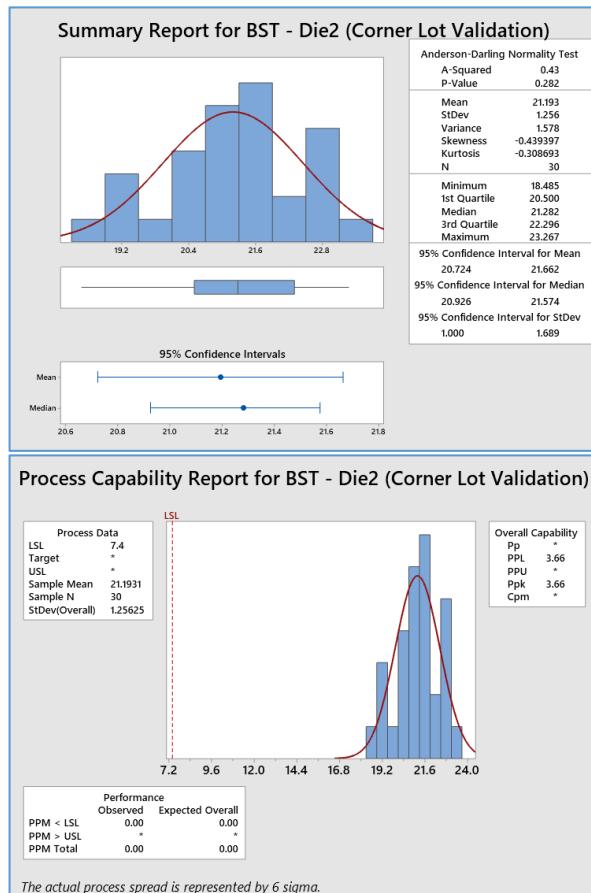


Fig. 29. BST of Die2 ASIC, with P-value = 0.282 and Ppk = 3.66.

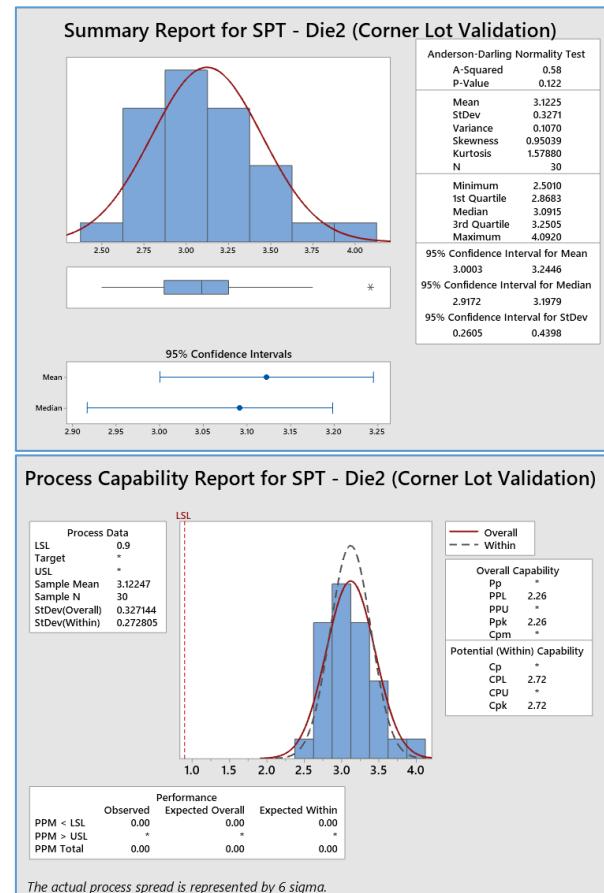


Fig. 30. SPT of Die2 ASIC, with P-value = 0.122 and Ppk = 2.26.

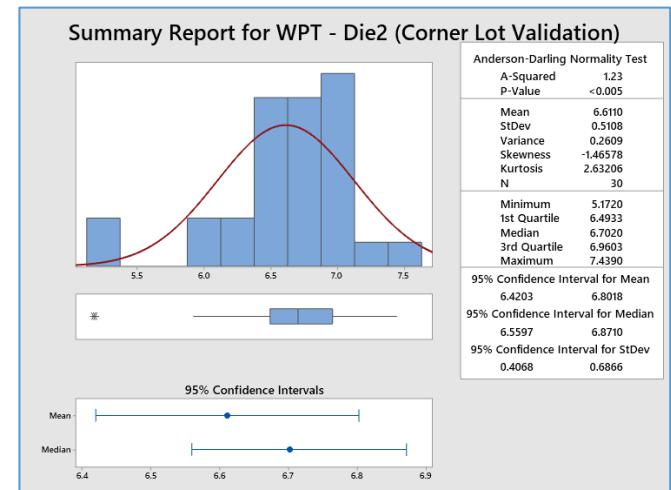


Fig. 31. Graphical summary of WPT of Die2, with P-value < 0.005, hence non-normal.

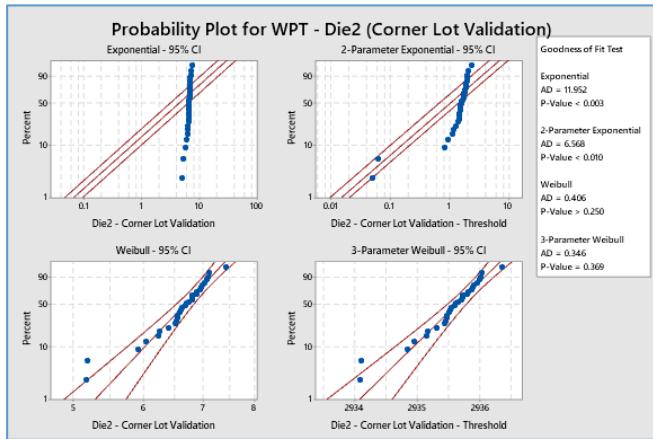


Fig. 32. Distribution identification for WPT of Die2, with Weibull of P-value > 0.250.

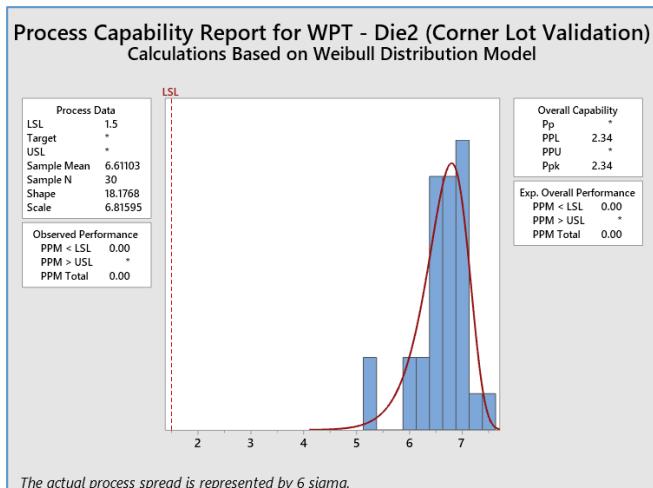


Fig. 33. Process capability of WPT of Die2, with Ppk = 2.34.

Package modeling and simulation was done to verify the effect of the adjusted die placement to achieve the 48.35 deg wire angle (C6Aalpha) in terms of the parasitic Resistance, Inductance, and Capacitance. Ideally, the result should retain or be comparable to that of the original MBD with wire angle of 46.32 deg. A 3D model is shown in Fig. 34.

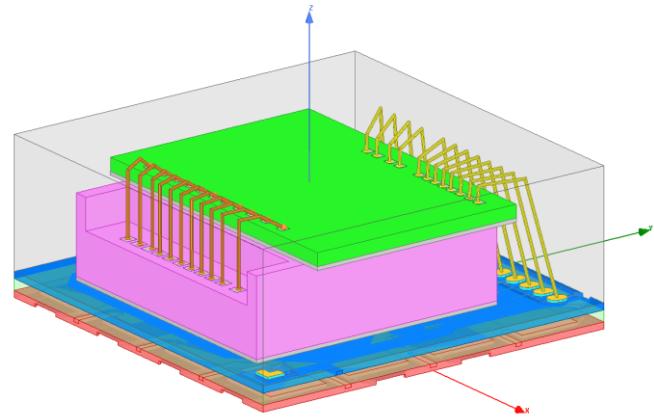


Fig. 34. Package 3D model of MEMS MY24 device.

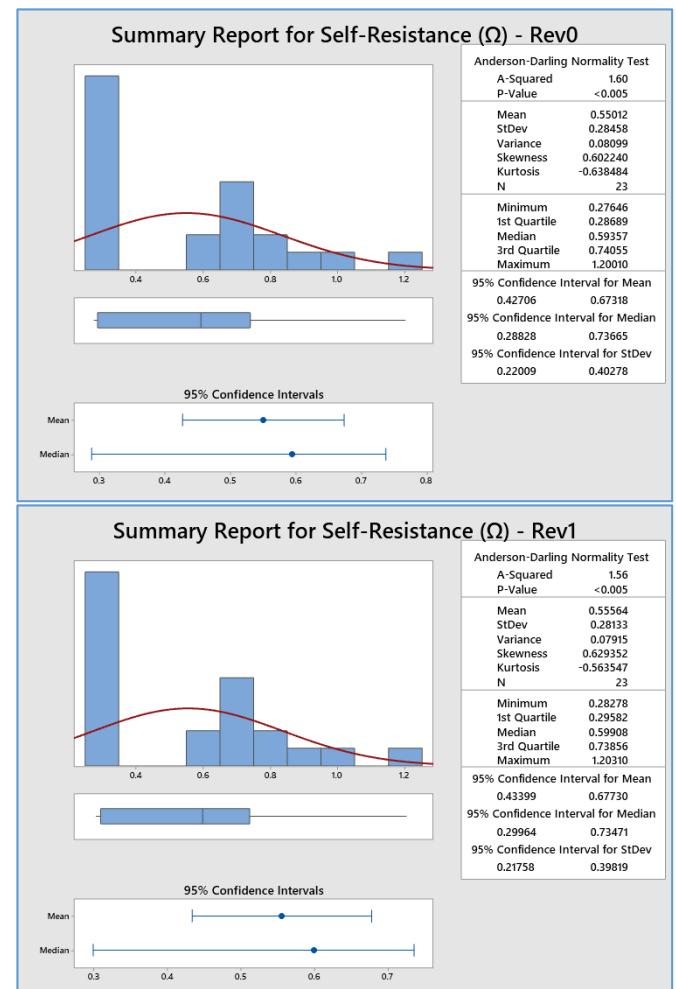


Fig. 35. Graphical summary of self-resistance showing non-normality for both models.

Results of self-resistance of both models (Rev0 and Rev1_adjusted die placement) were expected to be of non-normal distribution as each signal net has different

characteristic in terms of the signal length and width (wire + trace + pad), with 1 group of signals consisting of wires only. This also applies to self-inductance and self-capacitance values. Regardless, test for equal variances was done for non-normal data. And test for mean difference was completed assuming equal variances as presented in the succeeding figures.

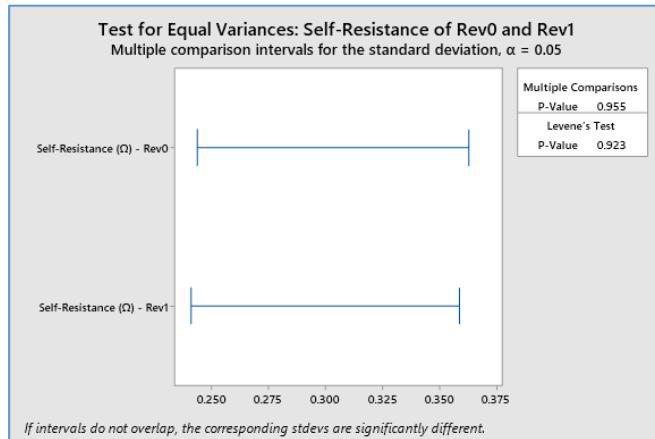


Fig. 36. Test for equal variances of self-resistance of the 2 models.

Since P-value using Levene's test is at 0.923 (and P-value > 0.05), hence, there is no significant difference in the standard deviations of self-resistance results between Rev0 and Rev1 models. 2-Sample T-test was done for the test for mean difference.

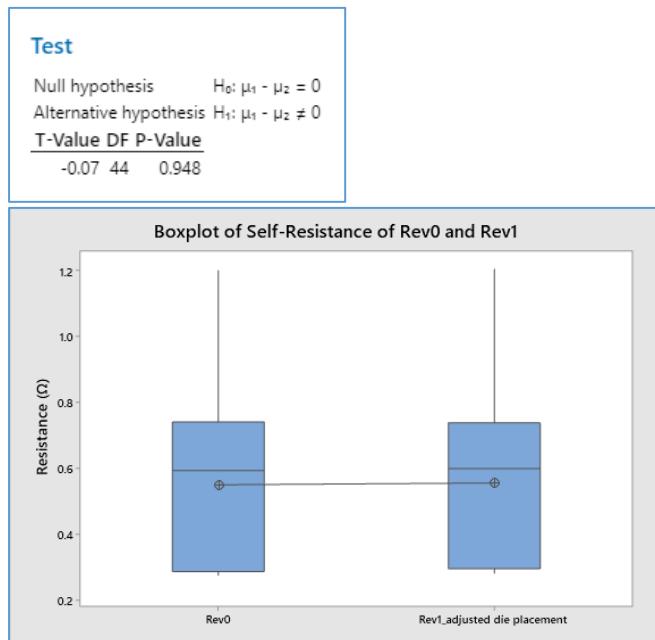


Fig. 37. Test for mean difference of self-resistance of the two models.

P-value is at 0.948, hence there is no significant difference in means of self-resistance results between Rev0 and Rev1 models.

As earlier mentioned, the analysis with non-normal data is the same for self-inductance and self-capacitance. Succeeding figures share the 2-Sample T-test conducted for the two models in terms of the inductance and capacitance.

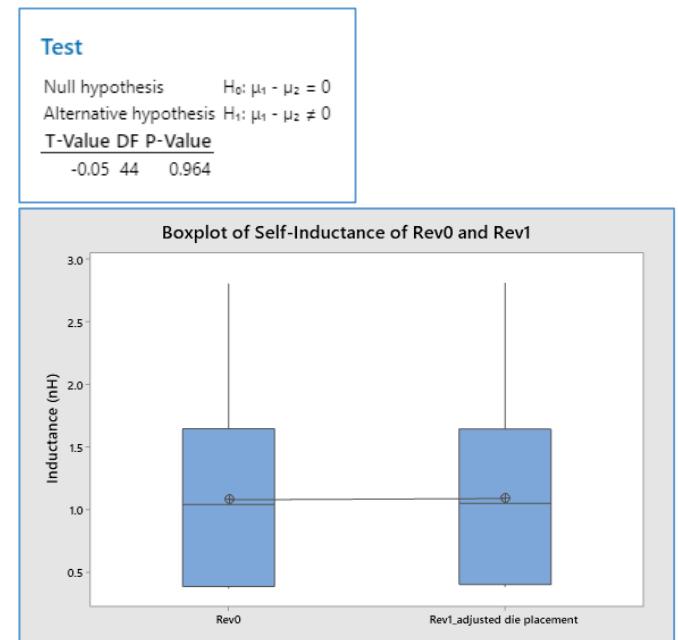


Fig. 38. Test for mean difference of self-inductance of the two models.

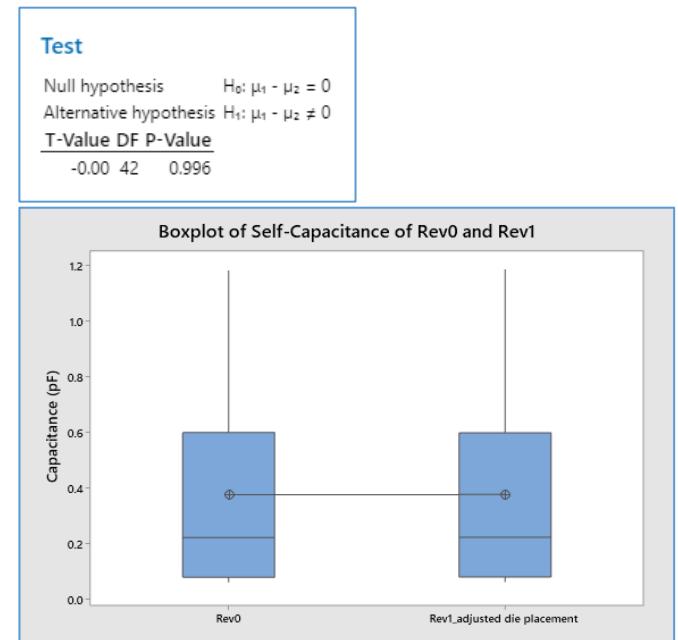


Fig. 39. Test for mean difference of self-capacitance of the two models.

Reliability tests were done on the device and it passed all package and electrical oriented tests, mechanical stress tests, and environmental stress tests. Fig. 40 shows the result of the electrical stress test.

Electrical stress test results								
N	TEST NAME	TEST DESCRIPTION	PREC	CONDITION/METHOD	STEPS	QUAL LOT1	QUAL LOT2	QUAL LOT3
6	HTOL	High Temperature Operating Life	Preconditioning	Ta = 125°C, Tj = 125°C Valid @ Max Op Voltage Reference specification IEC68-2-110B	100 H	PASS	PASS	PASS
					500 H	PASS	PASS	PASS
					1000 H	PASS	PASS	PASS
8	ESD	Electrostatic Discharge	NONE	HBM Voltage level up to +/-3000V (min target +/-750V) Reference specification ESD/ IEC68-2-209	FINAL	NONE	PASS	NONE
					FINAL	NONE	PASS	NONE
					MM Voltage level up to +/-200V (min target +/-750V) Reference specification IEC68-2-115	FINAL	NONE	PASS
9	LU	Latch Up	NONE	+/-100mA, 1.5Vdc, 1.5void Reference specification I _{LU} /JESD328	FINAL	NONE	PASS	NONE

Pass criteria are defined according to reliability plan QP000320CS2156_02.

The device passed all package and electrical oriented tests showing

- Offset is within +/- 40 mg
- Sensitivity is within +/- 1%

Fig. 40. Reliability test of electrical stress on the MEMS device.

With all the passing results, it successfully verified the mitigation of the wire-to-wire and wire-to-die shorting defects with the new optimized wire angle of 48 degrees.

5.0 CONCLUSION

The combination of risk analysis and assumptions for variability made the product robust for wire short occurrence of this MEMS device. The application of TRIZ tools, Monte Carlo Simulation Method, DFMEA and design rules review and update, the wire angle reduction significantly contributing to the elimination of wire short defect during wirebond process.

A new recommended die placement reference was generated, considering the results of the Monte Carlo Simulation and inputs from technical discussions. Ultimately, the wire angle parameter for top die to bond finger wirebonding was established and formulated from non-existing to 48 degrees steepest wire angle in absolute value with 90 degrees maximum, and applicable to die stackup of up to 235 μ m.

The full defect PPM monitoring of MY24 Argentera device was realized on large scale production. Fig. 39 shows results of no wire short occurrence, which is an indication of good manufacturing performance.

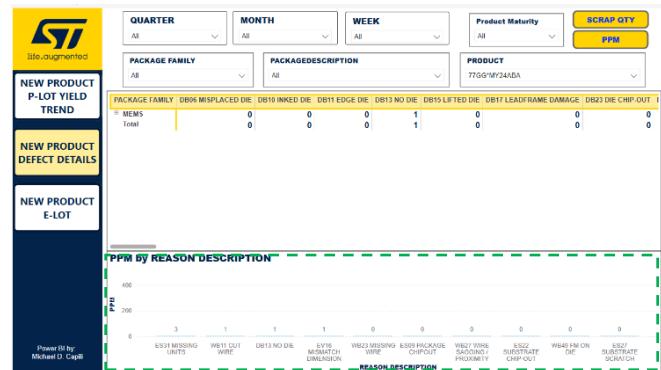


Fig. 39. Power BI dashboard illustrating MEMS MY24 Argentera production defect monitoring.

6.0 RECOMMENDATIONS

The successful implementation of new design rule applied to MEMS MY24, the prevention of such defect was then recommended to apply on the incoming MEMS devices. It is imperative to exert effort on analytical methods from a defect that is a combination of machine capability, process variability and package design rule. Recommendation to apply as well on the future MEMS product and similar structures. It will have an impact as well for the manufacturability as well productivity.

7.0 ACKNOWLEDGMENT

First of all, we thank our GOD ALMIGHTY for giving us the knowledge, strength, wisdom and giving us everyday blessings in our life. To our families who serve our inspiration on our career journey. Lastly to our colleagues from the New Product Introduction Department for supporting the project to become successful.

8.0 REFERENCES

- 0018063 61.0, Assembly and EWS Design Rules for Wire Bond Interconnect Dice, STMicroelectronics, January 2025.
- 7114456 42.0, Advanced Assembly and EWS Design Rules for Wire Bond Interconnect Dice, STMicroelectronics, January 2025.
- DM00686274 2.0, MEMS Sensor Assembly Rules Manual Full Mold Packages, STMicroelectronics, April 2024.
- Yeap, L. L., "Meeting the Assembly Challenges in New Semiconductor Packaging Trend," *34th IEEE/CPMT International Electronic Manufacturing Technology Symposium (IEMT)*, Malaysia, December 2010, pp. 1-5.

34th ASEMEP National Technical Symposium

5. Sumagpang Jr. A, et al., "Introduction of Reverse Pyramid Configuration with Package Construction Characterization for Die Tilt Resolution of Highly Sensitive Multi-Stacked Dice Sensor Device," *2020 IEEE 22nd Electronics Packaging Technology Conference (EPTC)*, Singapore, December 2020, pp. 140-146.
6. Mariano, R., et al., "Elimination of Non-Stick on Leads Defect Through Re-designed WCTP," *Journal of Engineering Research and Reports*, Vol. 12, No. 10, 2021, pp. 22-26.
7. Moreno, A., et al., "Enhanced Loop Height Optimization for Complex Configuration on QFN Device," *2020 IEEE 22nd Electronics Packaging Technology Conference (EPTC)*, Singapore, December 2020, pp. 182-184.
8. Saha, S., "Emerging Business Trends in the Semiconductor Industry," *Proceedings of PICMET '13: Technology Management in the IT-Driven Services (PICMET)*, San Jose, CA, USA, August 2013, pp. 2744-2748.
9. Tsukada, Y., et al., "Trend of Semiconductor Packaging, High Density and Low Cost," *Proceedings of the 4th International Symposium on Electronic Materials and Packaging*, Taiwan. December 2002, pp. 1-6.
10. Liu Y., et al., "Trends of Power Electronic Packaging and Modeling," *10th Electronics Packaging Technology Conference*, Singapore, December 2008, pp. 1-11.
11. Tan, C. E., et al., "Challenges of Ultimate Ultra-fine Pitch Process with Gold Wire & Copper Wire in QFN Packages," *36th International Electronics Manufacturing Technology Conference*, Malaysia, November 2014.
12. Sumagpang Jr. A, et al., "Introduction of Reverse Pyramid Configuration with Package Construction Characterization for Die Tilt Resolution of Highly Sensitive Multi-Stacked Dice Sensor Device," *2020 IEEE 22nd Electronics Packaging Technology Conference (EPTC)*, Singapore, December 2020, pp. 140-146.
13. Lall, P., et al., "Reliability of Copper, Gold, Silver, and PCC Wirebonds Subjected to Harsh Environment," *IEEE 68th Electronic Components and Technology Conference*, San Diego, California, USA; May 2018.
14. Qin, I., et al., "Wire Bonding Looping Solutions for Advanced High Pin Count Devices," *66th IEEE Electronic Components and Technology Conference (ECTC)*, 2016, pp. 614-621.

9.0 ABOUT THE AUTHORS



Frederick Ray I. Gomez is a Staff Engineer, Project Leader and a Member of Technical Staff. Currently, he is part of the Project Management Group handling MEMS NPI projects in STMicroelectronics Calamba.



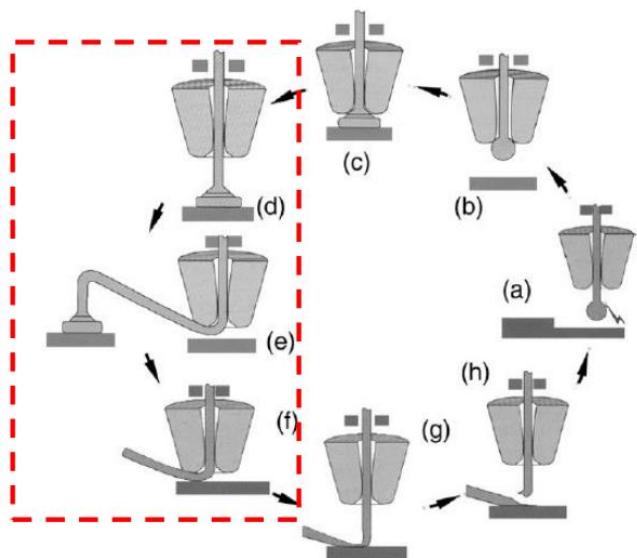
Freddie B. Folio is a Wirebond Process Development Sr. Engineer at New Product Introduction Department at STMicroelectronics, Inc. He is a graduate of BSECE under the ETEEAP program of the Manuel S. Enverga University Foundation. He is also a graduate of Bachelor of Science in Industrial Technology major in Electronics at the Batangas State University. He has been with STMicroelectronics for 21 years.



Anthony R. Moreno is an experienced Wirebond Process Technician of the under New Product Introduction Department at STMicroelectronics, Inc. He is a graduate of Bachelor of Science in Industrial Technology major in Electrical Technology at the Bicol State College of Applied Sciences and Technology. He has been with STMicroelectronics since 2016.

10.0 APPENDIX

Appendix A – Loop Process Step



Schematic of wirebond cycle: (a) electrical frame off process, (b) move to ball bond position, (c) ball bonding, (d) capillary lift, (e) looping, (f) move to wedge position, (g) wedge bonding, (h) wire tail formation.