PULSE TIME OPTIMIZATION FOR ENHANCED RELIABILITY CORRELATION OF BOND LINE THICKNESS TO THERMAL PERFORMANCE IN RF POWER GAN DEVICES

Kimberly P. Jardin
Roelof van der Berg
Floralyn T. Custodio
Eric G. Del Rosario

Quality & Reliability, New Product Introduction, Test Product Engineering
Ampleon Philippines, Inc., Binary Street, Light Industry and Science Park 1, Brgy. Diezmo, Cabuyao City, Laguna, Philippines 4025
Kimberly.Jardin@ampleon.com, Floralyn.Custodio@ampleon.com, Eric.g.delrosario@ampleon.com, Roelof.vanderberg@ampleon.com

ABSTRACT

One of the challenges in Gallium Nitride (GaN) is its thermal management, and a good die attach material like silver sinter is critical. Good quality is determined by visually checking its assembly workmanship and its functional correlation through thermal transient testing. Yet the thermal transient can be further improved for detection die attach anomalies like delamination during reliability testing and abnormalities at zero hour like voids or too thin bond line thickness (BLT).

Hence, a feasibility was conducted to determine the pulse time that would capture the die attach degradation of the GaN product using a transient thermal measurement.

The approach of the transient time and power optimization on (silver sintered) Die Attach and its thermal resistance performance on GaN is divided into three parts: assembly 1) sample building, 2) thermal characterization and setting the transient times and powers, and 3) testing the test program with different BLTs and at different read points in reliability tests.

Results showed that with shorter transients + increased power, an improvement in detecting zero-hour defects was noted and better detection of die attach degradation during life test/reliability testing.

1. 0 INTRODUCTION

Thermal transient testing is a semiconductor industry method of screening the die attach quality which indicates voids and or delamination, bond like thickness (BLT) out of defined criteria and deviating materials used such as in flanges.
In Final Test, thermal transient can be measured by analyzing the thermal behavior of the device by determining the voltage across the internal Schottky gate diode of the device, known as delta voltage (DvM).

For GaN devices, the Schottky gate diode acts as a temperature sensor and is used to detect a channel temperature increase after a heat transient. In Figure 1. shows how it is translated in DC Final Test, calculating the Delta Voltage between Forward Schottky Voltage at Cold and Forward Schottky Voltage at Hot. The magnitude of the delta is a measure for the increase in channel temperature.

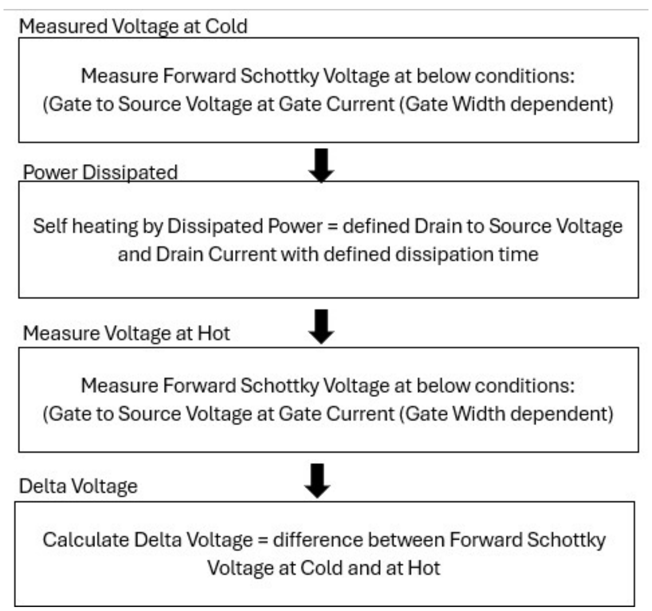

Figure 1. Simplified Block Diagram: Delta Voltage at Test

When the GaN device used in evaluation was subjected to transient thermal test, a significant shorter thermal time constant (RC), a measure of how a product responds to thermal changes like increase or decrease in temperature, was observed than the heat pulse used from the first test program generated. The RC is represented by the formula:

$$R\ (\text{die} + \text{die attach}) \times C\ (\text{die} + \text{die attach})$$

Where R is the thermal resistance and C the thermal capacitance.

Hence, a feasibility study was conducted to determine the pulse time that would capture the Die Attach degradation and bond line thickness variation of the GaN product using a transient thermal measurement.

By measuring the so-called structure function with the thermal transient test methodology (reference to JESD-51-12) the time constant for heating the die and die-attach can be determined. The time constant is used to set the minimum heating transient time in the final test program.

2. 0 REVIEW OF RELATED WORK

Measuring the thermal resistance of Gallium Nitride (GaN) devices is crucial for understanding their thermal performance, which is essential for reliable operation in high-frequency applications like RF Power devices.

Wang et al.1 investigated on thermal management in GaN High Electron Mobility Transistors (HEMTs) using various bonding method: (a) Face-up die bonding, (b) Flip-chip bonding with an on-chip heat-spreading layer, and (c) Flip-chip bonding with an optimized bump pattern. These three bonding methods resulted in different bond line thickness. Product thermal performance was determined through temperature rise. The temperature rise was measured for each bonding method under pulsed operation with time range from 1 µs to 9 µs. Results showed that method 2 and 3 configurations achieved a significant reduction in ΔT compared to method 1, indicating improved thermal management. The results indicated that optimizing pulse time and bond line thickness through advanced bonding methods significantly reduced thermal resistance, leading to enhanced thermal management in GaN HEMTs. However, this only covered zero-hour data and no further information on the die attach material used.

This study concentrated on the silver sintered die attach material, bond line thickness variation, different pulse time, functional test on both zero-hour and reliability.

3.0 METHODOLOGY

The approach of the transient time and power optimization on (silver sintered) Die Attach and its thermal resistance performance on GaN is divided into three parts: assembly 1) sample building, 2) thermal characterization and setting the transient times and powers, and 3) testing the test program with different BLTs and at different read points in reliability tests as shown on Figure 2.

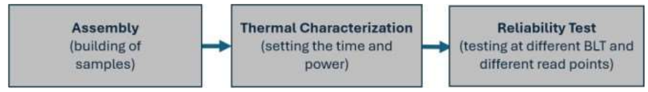

Figure 2. Experimental Setup of Pulse Time Optimization

3.1 Experimental Setup

3.1.1 Assembly Evaluation

To proceed with the pulse time optimization, an assembly evaluation was needed on a functional product comprised of five legs each with different BLTs ranging from 20 to 60um. Each BLT leg had 30 units. These BLT levels will be the basis in determining the assembly, test, and reliability performance.

3.1.2 Temperature/Thermal Characterization

The thermal transient measurements were done to set the minimum transient time and to scale the powers for the different transients. This procedure was executed according to JESD51-14.

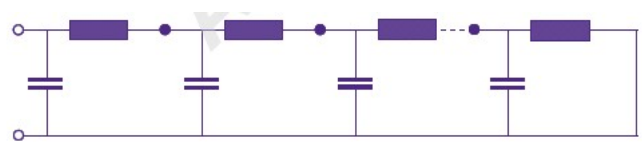

Figure 3. CAUER Type Representations of the Impedance of a Thermal One-Port

In thermal transient measurement, the device was heated with fixed power for 200s and after turning off, temperature cool down was measured by using the forward voltage Vf (5mA) of the Schottky diode. This was translated to temperature by using the calibration curve Vf (5mA) = f (T=20..100ºC) which was determined for the Schottky of the device under test. From the cooldown curve the structure function was determined by means of mathematical calculations/transformations explained in JESD51 document.

3.1.3 Functional Test

A product needs to ensure its high quality and functionality performance to have more extensive data on the pulse time optimization. Functional tests are used to test the integrity of the product using tester equipment. In this process, a dedicated test program was applied with a set of test parameters including different pulse times (ranging from 0.5ms to 10ms) to correlate with respect to different bond line thickness levels and with different die-attach degradations. Powers were scaled according to thermal transient resistance as determined with thermal transient characterization (reference to T3ster equipment).

3.1.4 Reliability Test

To address the pulse time optimization in different bond line thickness levels and how each level accelerates during product aging, a reliability test was performed. Temperature cycling (TC) and power cycling test (PCT) were used according to JEDEC standards JESD22-A104 and JESD22-A122, respectively. The thermal resistance was reviewed and analyzed per leg per reliability test read point.

3.2 Data Analysis

The thermal resistance values were plotted per reliability test read point using a reliability chart data. To correlate the thermal resistance behavior with respect to the pulse times per leg, a delamination check was performed on each reliability read point through the confocal scanning acoustic microscopy (c-SAM). Minitab software was also used in data analysis of the thermal resistance correlation with respect to the pulse times per bond line thickness (BLT).

4.0 RESULTS AND DISCUSSION

4.1 Transient Thermal Test (T3ster)

A sample with nominal bond line thickness was plotted in the T3ster graph.

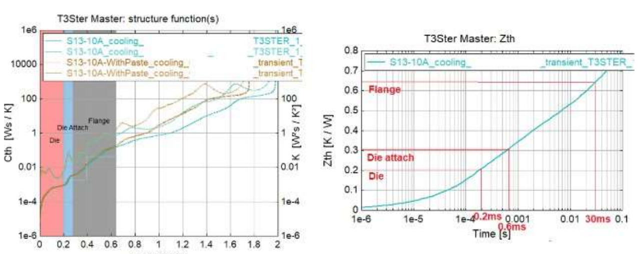

Figure 4. T3ster measurement of the sample with nominal bond line thickness

During the initial run, the Zth/Cth of die + Die Attach interface is 0.28 K/W and 0.005 Ws/K, respectively. The time constant (RC) is calculated by the product of Zth and Cth.

$$RC = Zth \ x \ Cth$$

The calculated RC of this level was 0.28 K/W x 0.005 Ws/K = 0.0014 sec (1.4 ms). This explains that at approximately 0.6 ms, the heat front reaches the back of the die attach and at 30 ms, the heat front reaches the back of the flange.

4.2 Pulse Time versus BLT

4.2.1 0.5 ms Pulse Time

The thermal resistance values were plotted against the BLT legs using the 0.5 ms pulse time and power of 466W and 542W on sections A and B, respectively, that were scaled from Zth curve of T3ster results.

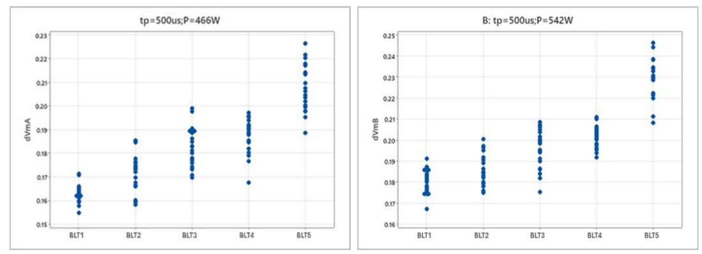

Figure 5. Thermal resistance vs BLT at 500 µs Pulse Time on Sections A (left graph) and B (right graph). BLT1 = 20+/-5um; BLT2 = 30+/-5um; BLT3 = 40+/-5um; BLT4 = 50+/-5um; BLT5 = 60+/-5um

A good correlation is observation with BLT is observed for both section A and section B for pulse time of 0.5ms.

By increasing the power for shorter pulse durations according to thermal transient resistance measurements, an improved correlation of 74% between thermal resistance and BLT was observed (see Fig. 7).

4.2.2 10 Milliseconds Pulse Time

The 10ms leg was plotted by thermal resistance against the BLTs as shown on Figure 6.

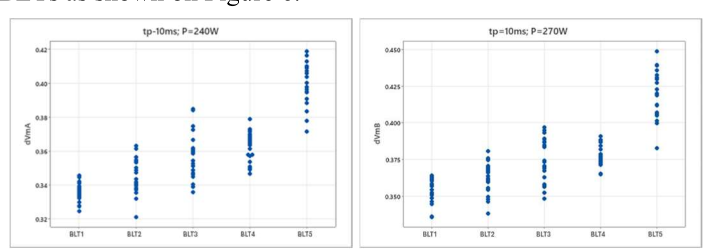

Figure 6. Thermal resistance vs target wet BLT at 10 ms Pulse Time on Sections A (left graph) and B (right graph). BLT1 = 20+/-5um; BLT2 = 30+/-5um; BLT3 = 40+/-5um; BLT4 = 50+/-5um; BLT5 = 60+/-5um

At 10 milliseconds pulse time, good correlation was also noted on the BLT. It explained that the pulse time ranging from 0.5 to 10 milliseconds is good for screening BLT and improvement on zero-hour defect screening. Moreover, there was an improvement in terms of monitoring the die attach degradation during life test/reliability testing.

Table 1. Dvm Shift Overview (%) of the Reliability Samples

Reliability Test	Read point	Results	delta forward voltage (Dvm) - 1ms		delta forward voltage (Dvm) - 5ms		delta forward voltage (Dvm) - 10ms	
			Ave (%)	Max (%)	Ave (%)	Max (%)	Ave (%)	Max (%)
Temperature Cycling TC -65/200°C	precon	0/30	0.1	0.9	0.3	1.2	0.2	1
	200 cycles	0/30	4.7	9.1	3.1	4.7	2.2	3.2
	500 cycles	0/30	19.6	29.5	10.3	13.8	6.8	8.9
	1000 cycles	22/30	37.4	59.8	17.7	25.1	11.3	15.8
	1500 cycles	30/30	59.5	101.7	27.8	43.3	16.8	24.8
	2000 cycles	30/30	65.9	109.5	28.7	43.1	17.1	24.1
Power Cycling Test (PCT)	5k cycles	0/5	3.4	4.1	3.2	4.4	2.4	3.4
	22k cycles	0/5	8.3	11.1	6.5	9.2	5.5	7.4
	38k cycles	0/5	9.2	13.9	7.1	10.6	6.1	8.3

Table 1 shows the Dvm overview of the reliability test samples in terms of the applied pulse times. It explained that the short pulses are more sensitive to die attach defects such as delamination whereas long pulses are closer to the channel case thermal resistance (Rth-channel) and show more effect of defect on temperature in application. When GaN devices are functional tested with RF signals, internal traps are filled and result to a shifted forward voltage curve, which results in a shift in the measured transient resistance. This shift however occurs to a comparable extent for all transients whereas a die-attach degradation will show a decreasing shift with the pulse times. Comparison of the shifts of the different transients supports in finding the root cause of shifts occurring during testing.

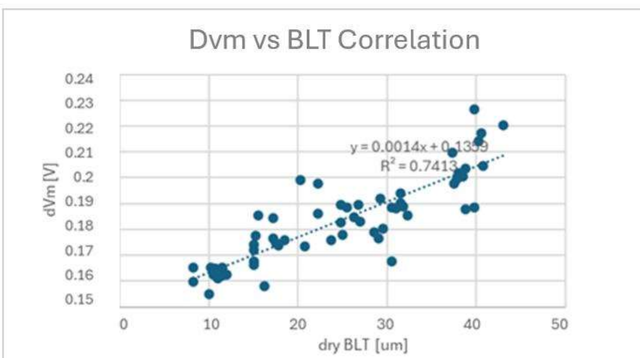

Figure 7. Linear Regression of the Dvm versus Dry BLT Correlation

To further analyze the relationship between the Dvm and the BLT, the data points of measured BLTs were plotted against the dVm measurement for linear regression. The results showed a direct relationship between the two variables. Using the linear regression $y = 0.0014x + 0.1359$, the BLT can be estimated based on the measured dVm.

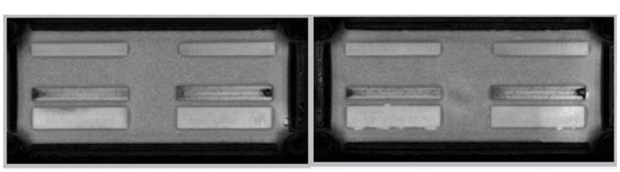
Figure 8. CSAM Images of the Reliability Samples

The CSAM images are indicative for the delamination occurring during temperature cycling for tests shown in Table 1.

The results gathered from the study were significantly higher compared to the study done by Wang et al with pulsed operation time ranging from 1 µs to 9 µs. The study conducted could be associated by the combination of the die attach material used, die attach technology, and package in contrast to was established from the previous study.

5.0 CONCLUSION

In summary, the pulse time of 0.5 to 10ms at 240 to 550 W utilized in this study was determined to be optimal with good reliability correlation with the bond line thickness and thermal performance on the RF Power GaN device. In addition, with shorter pulse times, an improvement in detecting zero-hour defects was noted and better detection of die attach degradation during life test/reliability testing.

6.0 RECOMMENDATIONS

The researchers recommended exploring how different pulse times can be used for other GaN and silicon products. A similar approach could also be used to define the pulse time based on different BLT levels. Additionally, a combination of different die attach material will also be beneficial on succeeding studies for more quantitative and qualitative results.

7.0 ACKNOWLEDGMENT

The authors would like to acknowledge the contributions of the following from different sites on this paper:
Nijmegen, Netherlands:
Peter Boltong (Principal Engineer, Test Engineering) Robert Koumkam (Principal Engineer, Test Engineering)
Henk Jan Ten Dolle (Senior Principal Engineer, Product Engineering)
Obet Sullera (Senior Manager, Project Management) Katherine Martinez (Senior Director, R&D Quality) Robbin Damen (Director, Product Engineering) Michael Asis (Director, Back-end Technology)

Ampleon Philippines:
New Product Introduction (NPI) Team
Adehl Arano (Director, NPI/Test Product Engineering) Mario de Vaan (Senior Director, Manufacturing Quality) Donald Locana (Senior Manager, NPI/Back-end Technology Quality)
Test Product Engineering Back-end Technology Team

Patrisha Louise Reyes (Jr. Engineer, Back-end Technology)
Norman Lanuza (Principal Engineer, Back-end Technology)
Management Team

8.0 REFERENCES

1. Wang et al, "Thermal Analysis of Flip-Chip Bonding Designs for GaN Power HEMTs with an On-Chip Heat- Spreading Layer ' , Micromachines, MDPI, 2022

9.0 ABOUT THE AUTHORS

Kimberly Jardin graduated from De La Salle University Manila with a bachelor's degree in chemical engineering. She also graduated from the Ateneo Graduate School of Business with a master's degree in business administration (MBA). She is currently working for Ampleon Philippines, Inc. as a Senior Quality Engineer in NPI/Back-end Technology Quality.

Roelof van der Berg is a Reliability Specialist with over 25 years of experience in the field of reliability engineering for (RF) power semiconductor devices and power electronics. He graduated from the University of Groningen with a master's degree in physics and has a bachelor's degree in Technical Physics from the H.T.S. Enschede.

Floralyn Custodio is a graduate of Bachelor of Science in Electronics and Communications Engineering from the University of Santo Tomas. She started her career in the semiconductor industry in 2003. She is currently working in Ampleon Philippines Inc. as a Senior Manager in Test Product Engineering Department and mainly handling the development and improvement of different GaN products.

Eric G. Del Rosario is a graduate of B.S. Electronics and Communications Engineering at Manuel Enverga University Foundation in Lucena Quezon. Currently working as NPI Engineer in Ampleon Philippines Inc.