OPTIMIZING RETEST RATES IN TSSOP FOR SUSTAINABLE MANUFACTURING

John A. Manalo
Mark Joshua Velasco
Frank Carias

Test Operations
Allegro MicroSystems Philippines, Inc. 4756 Sampaguita St., Marimar Village 1, Sun Valley, Parañaque City
jamanalo@allegromicro.com; mavelasco@allegromicro.com; fcarias@allegromicro.com

ABSTRACT

High Retest rate is a serious problem affecting productivity and quality. The goal of this project was to reduce the retest rate of Thin Shrink Small Outline Package (TSSOP) devices by at least 30%, aiming to improve manufacturing efficiency and reduce operational costs. To achieve this, a structured problem-solving approach was employed, leveraging tools such as (1) brainstorming sessions, (2) Why-Why Analysis, (3) Ishikawa (Fishbone) Diagrams, (4)GEMBA Walks, and (5) T.I.M.W.O.O.D.S. waste reduction framework.

This paper revealed the results of the investigation contributing to high retest rates: (1) Poor contact due to dirty pins, (2) worn-out contact pins, and (3) misalignment leading to multiple testing failures such as alarming readings and repeated Open/Short (OS) test rejects. These issues caused bottlenecks and unnecessary retesting across multiple production lines.

In response, several corrective and preventive actions were implemented. An Auto-Insertion Counter program was embedded to track the lifespan and performance of contact pins, ensuring timely replacement. An Out-of-Control Action Plan (OCAP) was also introduced to maintain cleanliness of test interface components. Additionally, program optimization was carried out to reduce false Open Short and alarm triggers.

As a result of these initiatives, a 60% reduction in retest rate was achieved—far exceeding the original 30% target. This outcome underscores the effectiveness of using comprehensive root cause analysis and structured problem-solving tools in addressing manufacturing challenges. Proper identification of the root causes enabled targeted solutions, ultimately enhancing overall test efficiency and quality.

1.1 Introduction

In the increasingly competitive landscape of semiconductor manufacturing, operational efficiency 0is paramount to maintaining product quality, customer satisfaction, and cost-effectiveness. One of the key performance indicators used to assess manufacturing productivity is Overall Equipment Effectiveness (OEE), specifically, Availability. A high OEE reflects streamlined processes and minimal production losses, while a low OEE signals inefficiency that must be addressed to ensure sustainable operations.

This study investigates the persistent issue of low Availability in the testing phase of Thin Shrink Small Outline Package (TSSOP) products, with a particular focus on the impact of high retest rates. Retesting not only increases cycle time and equipment usage but also leads to higher operational costs and resource consumption.

Through a detailed analysis, this study identifies the primary root causes contributing to the elevated retest rates, which include:

1.1.1 High Open/Short Failures – These failures are indicative of poor electrical continuity or short circuits, often occurring due to unstable connections or component defects.

1.1.2. Alarm Failures Due to Contact Issues – Inconsistent or weak contact between the test interface and device under test has resulted in erroneous alarms and unreliable test results.

1.1.3. Misaligned Contact Caused by Plunger Issues – Mechanical misalignment in the contact mechanism, particularly involving plunger wear or improper calibration, has further compromised testing accuracy and consistency.

1.1.4. Off-State Leakage Failures – These failures occur when leakage current is detected under conditions where the device should exhibit high impedance. Causes include poor contact stability, environmental noise, or suboptimal test program settings.

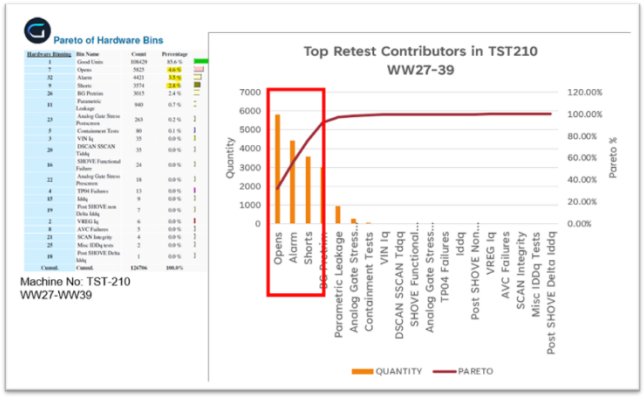
The objective of this research is to systematically examine these failure mechanisms, quantify their impact on Availability, and propose targeted improvements to enhance test yield and reduce retesting. By addressing these key issues, this research aims to contribute to the restoration and improvement of Availability in TSSOP final test operations, with the goal of achieving a 30% reduction in retest rate,

enhancing both operational performance and product reliability.

1.2 Background of the Study

In semiconductor manufacturing, particularly in the final test stage, achieving high Availability is crucial for maintaining throughput, quality, and profitability. Availability is one of the factors in OEE. In recent years, there has been increasing pressure to optimize Availability across all package types, including Thin Shrink Small Outline Package (TSSOP) products, which are widely used in automotive, consumer, and industrial electronics due to their compact form factor and electrical performance.

However, despite advancements in automation and process control, certain manufacturing lines have experienced persistently low Availability, primarily attributed to high retest rates during final testing. Retesting not only reduces effective throughput but also increases equipment wear, labor costs, and the risk of undetected defects due to test fatigue or variability. See Figure 1 for the retest contributors at Allegro.



Figure# 1: Retest rate contributors

Preliminary data and root cause analyses indicate that open/short failures, alarm failures due to poor contact, and mechanical misalignments caused by plunger issues are the leading contributors to these retests. These issues often stem from factors such as test socket degradation, improper handler alignment, or insufficient maintenance routines.

This study was initiated in response to ongoing production challenges in TSSOP lines, with the goal of identifying the exact failure mechanisms, quantifying their effect on OEE, and recommending corrective actions that can restore optimal efficiency and test reliability.

1.3 Objective of the Study

The primary objective of this study is to analyze and address the root causes of High Retest Rates in the final test stage of TSSOP-packaged semiconductor products. Excessive retesting has led to increased equipment downtime, extended cycle times, and higher operational costs—factors that negatively affect overall productivity and test efficiency.

This study aims to reduce Retest rates by identifying and mitigating the major contributors at Final Test. The specific objectives are to:

1.3.1 Investigate the root causes of Open/Short failures, which significantly lower first-pass yield and contribute heavily to test inefficiencies.

1.3.2. Analyze alarm failures related to contact integrity issues, including poor electrical connection between the device under test (DUT) and the test socket.

1.3.3. Examine Off-State Leakage failures and determine whether they are driven by contact instability, test environment variability, or test system limitations.

1.3.4. Evaluate mechanical misalignments—particularly those caused by plunger wear or improper alignment—that affect consistent contact during testing.

1.3.5. Incorporate test program optimization strategies, such as refining parametric limits and implementing improved test sequencing or soak routines, to minimize Off-State Leakage false failures.

1.3.6. Quantify the contribution of each failure type to overall retest rates and evaluate their cumulative impact on availability.

1.3.7. Implement corrective and preventive actions to improve contact reliability, mechanical alignment, and test program accuracy.

As a measurable goal, the study targets a 30% reduction in the overall retest rate for TSSOP products. Achieving this objective will result in improved test floor efficiency, higher first-pass yield, reduced cycle time, and increased equipment availability—ultimately enhancing the operational performance of the final test process.

1.4 Scope and Limitations

1.4.1 Scope:

- This study focuses specifically on the final test process of TSSOP-packaged semiconductor devices within a single production facility.
- The investigation includes analysis of test yield, OEE components (availability, performance, quality), and retest data over a defined period.
- Root cause analysis is confined to electrical test failures, with emphasis on open/short, alarm failures, and mechanical misalignment due to plunger/contact issues.
- The study explores both technical (equipment and hardware) and procedural (test setup and handling) factors that contribute to high retest rates.

1.4.2 Limitations:

- The study does not cover upstream processes such as wafer probing, die attach, or mold that may indirectly

influence test performance.
• The analysis is limited to TSSOP products and may not fully generalize to other package types like QFN or BGA.
• Equipment and failure data are based on a specific set of handlers and test systems, which may vary across different production sites or toolsets.
• Time constraints limit the investigation to a retrospective data review and a small set of controlled experiments; long-term validation of corrective actions is beyond the current study scope.

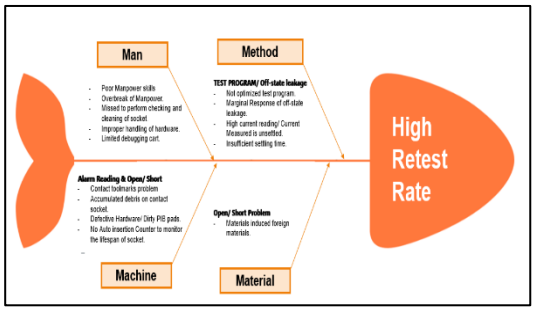
EXPERIMENTAL SECTION

2.1 Methodology

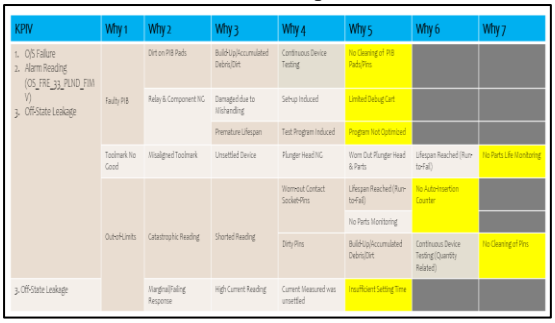
This study aims to reduce the retest rate of ICs in the TSSOP category by 30%, specifically focusing on the 814071TLV product. An experimental approach was employed to identify root causes of high retests and implement targeted process improvement.

2.2 Root Cause Analysis

Based on the engineering expertise and experience of each team member, a structured brainstorming session was conducted to identify potential causes contributing to the High Retest rate observed in the TSSOP 814071TLV package. The outcomes of this collaborative analysis were captured in a fishbone (Ishikawa) diagram, and 5 why analysis, which was developed and finalized by the team as shown below:



Figure# 2: Ishikawa diagram underlining potential sources of the problem



Figure# 3: 5 why analysis underlines potential sources of the problem

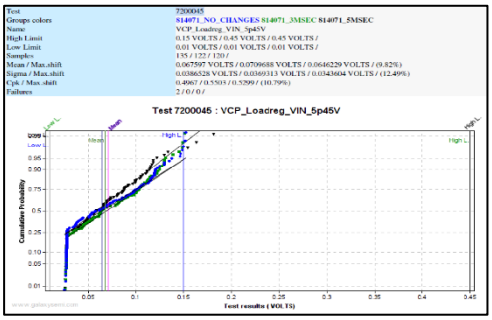
2.3 Procedure

The following outlines the experimental approach undertaken to reduce the retest rate for product 814071TLV.

2.3.1 Program Optimization

This phase involves the program optimization for the following parameters:

- **VCP_Loadreg_VIN_5p45V** – marginally failing at upper limits, the team optimize this parameter by adjusting the limits from 0.15 volts to 0.45 volts limits.



Figure# 4: VCP_Loadreg_VIN_5p45V Plot distribution

- **Output_Leakage_MISO_0Volt** – increase the settling time from 2ms to 3ms prior forcing voltage condition of MISO pins.

```
//*************************************************************
//Output_leakage_MISO_0V.
//*************************************************************

    dpinviset( "MISO", DPIN_FV, 0.0, DPIN_8V, DPIN_8UA, DPIN_CLAMP_OFF, DPIN_CLAMP_OFF, MS_ALL );
    lwait ( 0 MSEC); //from lwait (2 MSEC); mavelasco 101823
    dpinmi( "MISO", 52, 10.0, MS_ALL );
    groupgetresults( MISO_Leakage_0V, NUM_SITES);
    msScaleDataAll(1E3, MISO_Leakage_0V, NUM_SITES); //in uA
    msLogResultAll(DSIndex++, MISO_Leakage_0V, NUM_SITES);
```

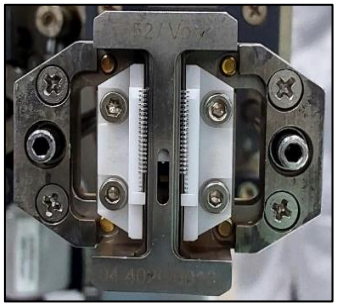
Figure# 5: Output_Leakage_MISO_0Volt settling time improvement

2.3.2 Embedded Auto Insertion Counter

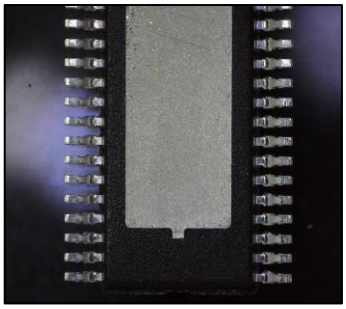
Embed an auto insertion counter into test program to track contact socket insertion during production run, aiding in monitoring contactor usage and tool lifespan.

2.3.3 Plunger Head Alignment

Plunger Head lead support alignment in HSI, checking of contact marks alignment and plunger head condition prior production run.



Figure# 5A: Plunger Head



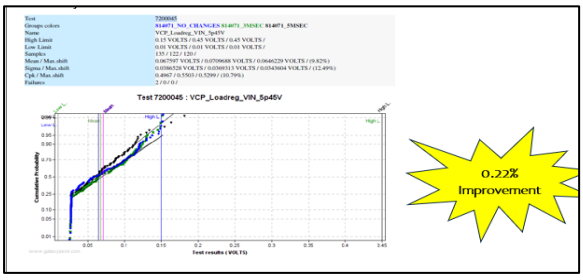
Figure# 5B: Sample Contact Marks

3.0 RESULTS AND DISCUSSION

3.1.1 Test program optimization through limit adjustment

Limits adjustment of test parameter VCP_Loadreg_VIN_5p45V which has a marginal reading condition in upper limits was changed from 0.15V to 0.45V.

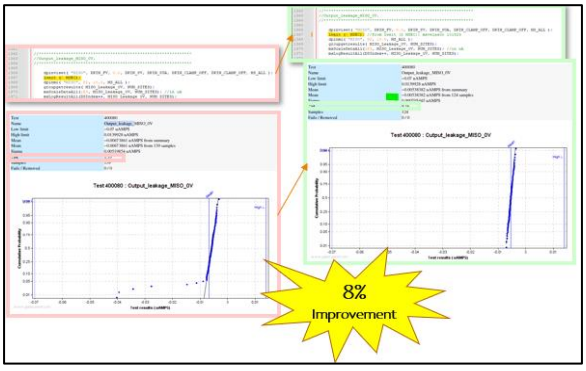
Results: 0.22% yield improvement from 5.71% to 5.49%



Figure# 6: VCP_Loadreg_VIN_5p45V Plot distribution

3.1.2 Test program optimization through settling time optimization

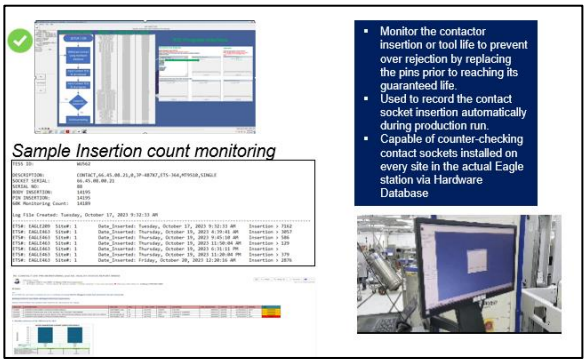
Characterization of settling time on forcing voltage condition of MISO pin from 2ms to 3ms.
Results: 8% yield improvement from 6.21% to 5.71% retest rate, Cpk also improved to 9.16.



Figure# 7: Output_Leakage_MISO_0Volt settling time improvement

3.1.3 Embed auto insertion counter

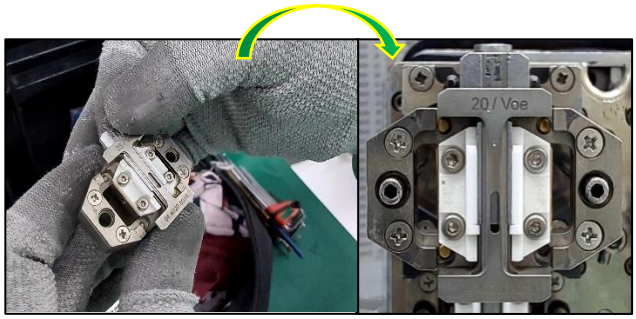
Embedded automated insertion count in test program



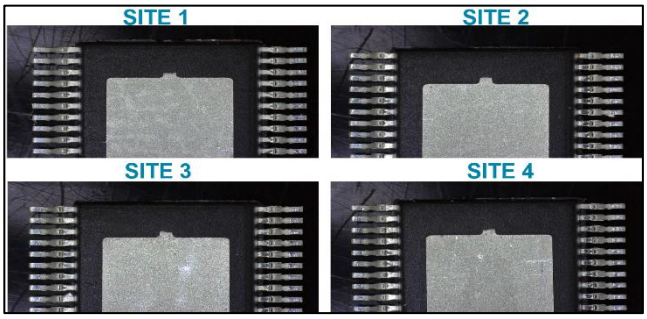
Figure# 8: Embedded Auto insertion counter

3.1.4 Plunger Head Alignment

Introduced contact marks and alignment qualification through the usage of "lead support alignment jig" during Handler Set up Inspection process.
Results: Set up qualifications to determine the contact marks condition prior test

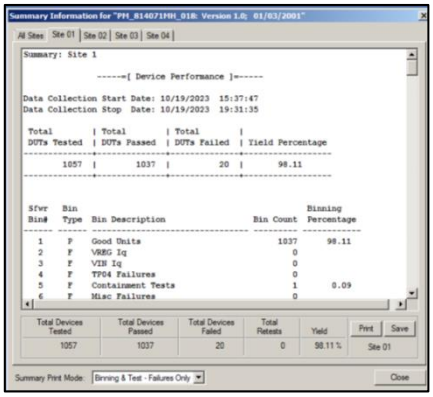


Figure# 9: Alignment Jig 5.5 mm



Figure# 10: Good contact alignment

3.2

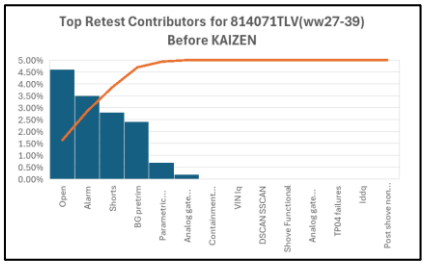


Validation and Results

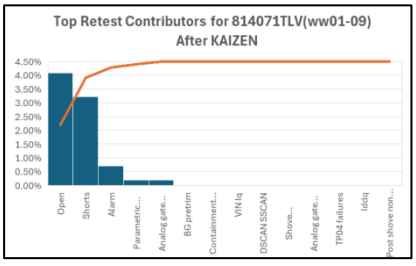
3.2.1 Improvement Impact – Failure rate reduction.

See below Failures Rates Before and After Kaizen

Figure# 11: Failure Rate Before



Figure# 12A: Failure Rate Kaizen



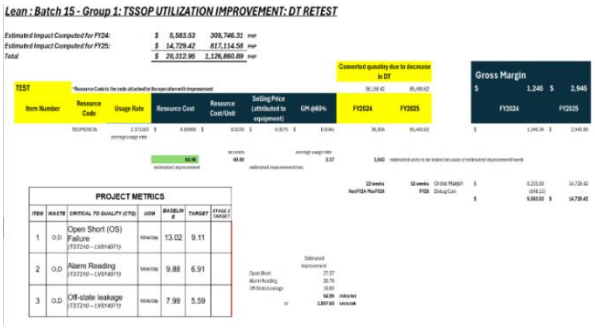
Figure# 12B: After Kaizen Pareto

Item	Focus	From	To	Gain
1	Open/ Short	7.4%	7.3%	0.1%
2	Machine Alarm Reading	3.5%	0.7%	2.8%
3	Off State Leakage	0.7%	0.2%	0.5%
	Total	11.6%	8.2%	3.4%

Figure# 13: Yield Improvement

Test yield after the implementation of methodology.

3.2.2 Improvement Impact - Cost savings



4.0 RECOMMENDATIONS

The Authors would like to share the benefits this paper achieved and to fan out this project to other devices experiencing High Retest Rates.

5.0 ACKNOWLEDGEMENT

Sincere gratitude is extended to the following people for their contribution to the completion of this project;

• Neil Sullera, Equipment Engineering Department Manager
• Maricar Lopena, Moises Apigo, Beverly Madural, Rovelle Overa, Foilan Gandoza, Ailyn Macalalad and Vincent Rosqueta for the help in Data collection and analysis and conducting frequent line compliance check.

6.0 CONCLUSION

Overall, this study showed that (1) Optimizing Test Program (Limit Adjustment and Settling time), (2) Auto Insertion Counter in the Test Program and (3) Lead Support Alignment Jig will contribute to Retest Rate Reduction. Other activities such as mishandling elimination on Product Interface Board and predictive maintenance on plunger assembly also helped in this improvement.

7.0 ABOUT THE AUTHORS

John A. Manalo, PhD is the head the Quality Control of Allegro Microsystems Philippines. He's also an Associate Professor at College of Business and Accountancy, De La Salle University-Dasmarinas Cavite.

Mark Joshua Velasco is a graduate of BS Electronics & Communications Engineering at TUP-Manila. He is currently the Manufacturing Product Engineering Senior Engineer in charge of legacy products.

Franklin Carias is a graduate of BS Electronics & Communications Engineering at Central Philippine University-Iloilo. He is currently the IC Test Sustaining Supervisor.