BAKE SETTINGS OPTIMIZATION FOR PROCESSING TIME IMPROVEMENT ON 50-WATT GAN DFN PACKAGE TYPES

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ABSTRACT

In the semiconductor manufacturing industry, product cost serves as a critical determinant of a company's competitive advantage. Processing time, or the time it takes to complete a step in the whole production flow, is a factor that affects the throughput time (TPT) which in turn influences the cost of the final product – the higher the TPT, the higher the cost will be to build a product. Therefore, releasing new devices with optimum processing time on each step is crucial to achieve high performing products in the least amount of time possible.

Applying structural similarity is widely popular in the semiconductor industry as it helps in reducing the efforts in qualifying new products using already available settings. Doing so, however, may lead to missing out on process improvements that will be more beneficial in the long term.

This study presents why Bake setting of the new 55W gallium nitride dual flat no-lead (GaN DFN) 7×6.5mm device, which was inherited from the 110W GaN quad flat no-lead (QFN) 8×8mm package, was challenged; and how the team achieved a 66.7% processing time improvement on the said step through Cumulative Distribution function (CDF) and Distribution Shift Analysis (DSA) of the product's RF and DC performance at varying conditions.

1. 0 INTRODUCTION

Processing time refers to the time consumed on a single step or equipment to complete the lot per defined number of pieces.

This is critical for productivity; faster processing time means higher output, translating to lower cost. However, there are various factors affecting the processing time such as device complexity, assembly and test flows, and firewall introduction among others.

For the development types (i.e. new technology, new die, new package), there would be instances that certain flows/settings are derived from already existing devices, but this might lead to a higher processing time.

Like with the GaN DFN 55W new device type that used the 6-hour Bake setting of GaN QFN 8×8mm with the same die technology, which is 300% higher than the 2-hour bake typically used in other GaN DFN packages with an older die technology. Figure 1 shows the percentage delta of processing time per process.

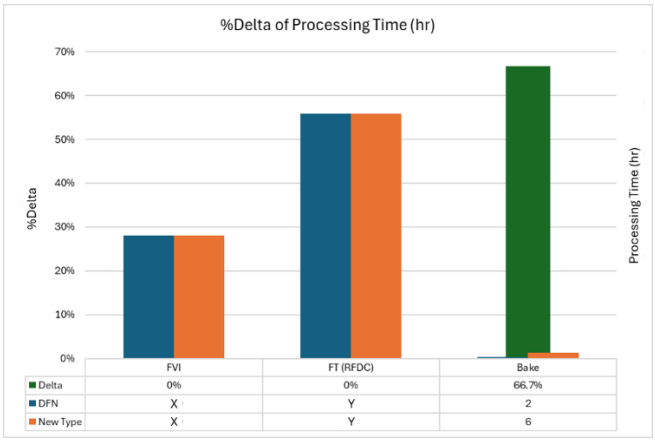

Figure 1. % Delta of Processing Time per Process

The paper evaluated different baking settings to reduce processing time without compromising electrical and RF performance due to inherent trapping on GaN.

2. 0 REVIEW OF RELATED WORK

Different packages have different levels of moisture sensitivity. The higher the amount of moisture inside a package, the higher the thermomechanical stress inside the package during board mounting will be. These stresses are brought about by the rapid vaporization of the trapped moisture and can be large enough to fracture the package during board mounting.[1]

Moisture-sensitive devices are baked and vacuum-sealed inside a moisture barrier bag prior shipment to minimize their tendency to exhibit popcorn cracking during board mounting. Users of such devices are likewise required to board mount the units within a prescribed period after the bag has been opened. Failure to do so calls for a re-bake of the units prior to board mounting. [1]

However, baking is critical to ensure moisture-sensitive devices will have no issues on package such as the popcorn effect as outlined in IPC/JEDEC J-STD-033. Trapping related issues on GaN which might affect RF and electrical performance were not evaluated and were included in the study of the paper.

3.0 METHODOLOGY

The paper evaluated different conditions on bake process to determine optimum conditions with lower processing time while maintaining electrical and RF integrity as non-baking causes performance shifts due to inherent GaN trapping related issues.

3.1 Materials

A mix of known good and reject units with a total of 140 pieces were used for the evaluation. Same set-up (tester, device interface board, oven for baking) was used for the evaluation and validation runs.

3.2 Procedure

The set of samples was tested initially to get a baseline of the RF and electrical performance. Afterwards, the devices were subjected to retests at different bake settings and time intervals as summarized in Table 1. Figure 2 illustrates the sequence of retest per condition.

Based on the evaluation of multiple bake settings and waiting time intervals, validation runs were executed.

Table 1. Evaluation Conditions

Condition	Qty	Temperature	Soak Time	Staging Interval
0HR	140pcs	ambient	-	-
125C_10HRS	140pcs	125°C	10 hours	-
125C_1HR	140pcs	125°C	1 hour	-
165C_1HR	140pcs	165°C	1 hour	-
WAITING_1_DAY	140pcs	ambient	-	1 day
WAITING_7_DAY	140pcs	ambient	-	7 days

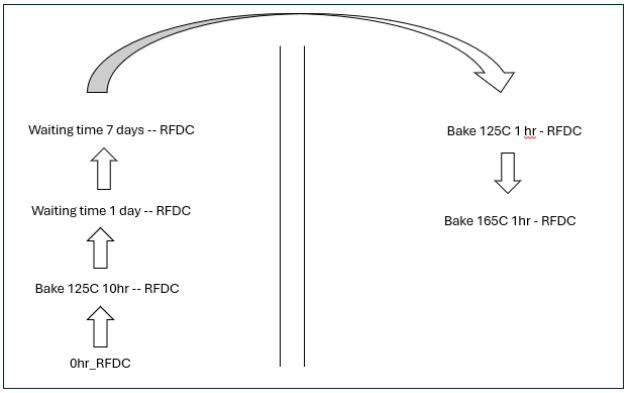

Fig. 2. Bake Settings and Waiting Time Intervals.

3.3 Data Analysis

For the data analysis, Cumulative Distribution Function and Distribution Shift Analysis were used.

Cumulative Distribution Function (CDF) charts help in defining the shape and normality of distributions, as well as the presence and location of outlier points. By default, the y-axis has a Gaussian (normal) scale; if a series in the chart follows a normal distribution, points of the series appear in a straight line. In case out-of-limits points are present, the area between the limit and the furthest out-of-limit point is shaded[2] (see Fig. 3).

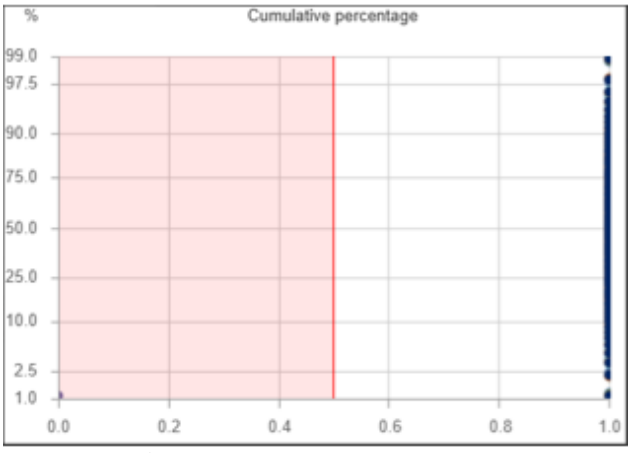

Fig. 3. Sample of Cumulative Distribution Function Graph.

For the validation runs, distribution shift analysis was used.

The analyses in the Distribution Shift Analysis report are based on robust statistics. For each parameter, the median and sigma, a robust estimate of the standard deviation (inter-quartile range / 1.35) is compared between both scopes (reference population/new (evaluation)). It is used to identify the parameters which significantly shift between two scopes.[2]

For the Distribution Shift Analysis, it checks the median shift and sigma ratio. Formulas and criteria for median shift and sigma ratio are shown below:

Formula:

$$\text{Median Shift} = \frac{\text{Median}_{(new)} - \text{Median}_{(ref)}}{\text{Robust Sigma}}$$

$$\text{Sigma Ratio} = \frac{\text{Robust Sigma}_{(new)}}{\text{Robust Sigma}_{(ref)}}$$

Criteria:

Median Shift: < +/-1.5 (absolute terms)
Sigma Ratio: 0.5-2.0

The Median Shift analysis is a scatter plot in which each point represents a parameter. The y axis displays the difference in median normalized by sigma of the reference population (ref). The x axis displays the CpK of the second population.[2]

The Sigma Ratio analysis is a second scatter plot in which each point represents a parameter, and where the x axis displays the CpK of the second population (2nd pop). Here, the y axis displays the ratio of the 2nd population sigma and the reference population sigma for each parameter. [2]

Parameters failing the median shift and sigma ratio criteria will be checked including the CpK of the 2nd population. Figs. 4 and 5 show sample median shift and sigma ratio graphical representations.

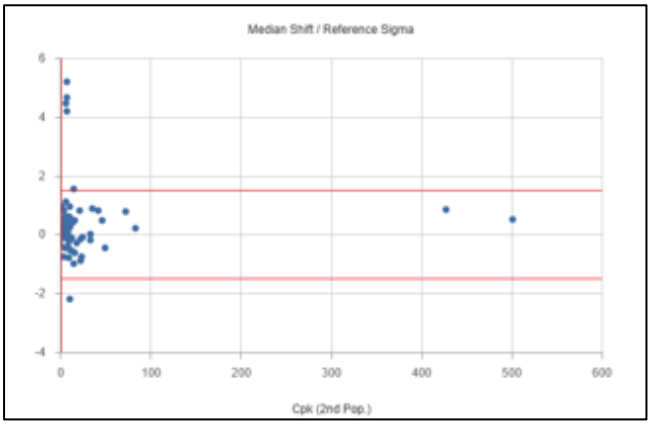

Fig. 4. Sample Median Shift.

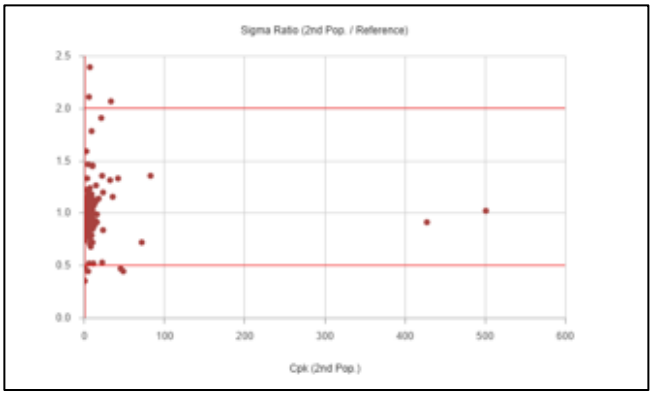

Fig. 5. Sample Sigma Ratio.

4.0 RESULTS AND DISCUSSION

Results will be in three parts: (1) Part 1 is on the evaluation done on different bake settings and waiting time interval; (2) Part 2 is on the validation runs for the optimized bake settings in comparison with the used bake settings; and (3) Part 3 is for recalculating the processing time.

This section highlights how optimized bake settings significantly improved efficiency by reducing processing time, all while maintaining electrical and RF integrity.

4.1 Cumulative Distribution Function Graphs of different Bake Settings and Waiting Time Interval

In total, 140 units coming from different diffusion (mixed of passed and rejects) were processed in RFDC on different bake settings and waiting time intervals.

Based on CDF graphs comparable response and or minimal shifts observed in RF performance (see Fig. 6). No significant differences were observed on different bake settings and CpKs are greater than 1.67 as shown on Table 2.

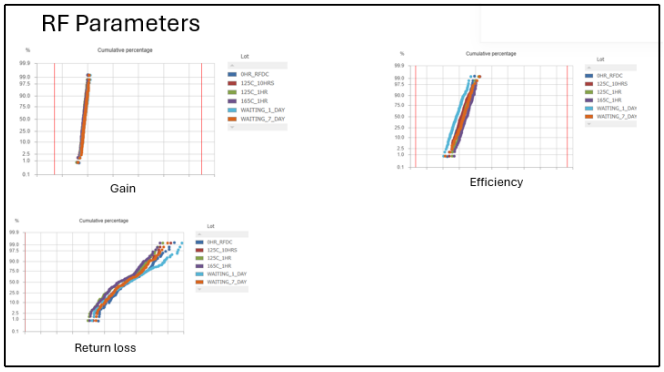

Fig. 6. CDF graphs on RF performance.

Table 2. CpK on RF Performance

	CpK		
Condition	Efficiency	Gain	Return Loss
0HR_RFDC	2.838794	6.134128	1.957817
125C_10HRS	2.801460	5.129656	1.991032
125C_1HR	3.277430	5.258481	1.780216
165C_1HR	3.321091	5.110206	1.855858
WAITING_1_DAY	2.509095	4.853347	1.588786
WAITING_7_DAY	2.862443	5.241898	1.954968

As illustrated in Fig. 7, CDF graphs indicated no significant variation in overall electrical performance except for the threshold voltage. A noticeable increase in threshold voltage was observed for the runs with different waiting time intervals while lower for runs with multiple bake settings.

Higher temperature 165°C 1 hr. or longer soaking time 125°C 10 hrs. did not improve recovery of trapping related parameters such as gate leakage where rejects are still the same as with the 0hr.

On Table 3, CpKs are high as well for electrical performance of different settings.

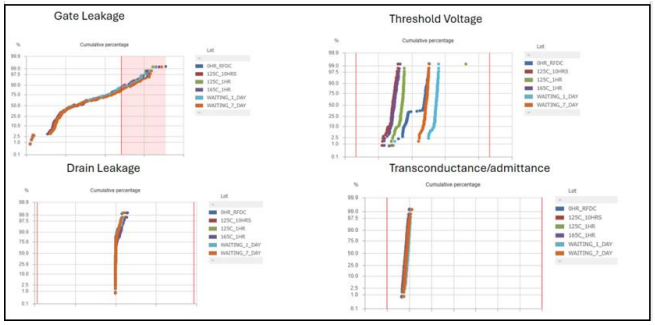

Fig. 7. CDF graphs on electrical performance.

Table 3. CpK on Electrical Performance

	CpK			
Condition	Transconductance	Drain_Leakage	Gate_Leakage	Threshold_Voltage
0HR_RFDC	4.352108	21.612993	12.438815	2.308261
125C_10HRS	3.186151	11.349874	10.885096	4.233028
125C_1HR	3.044916	13.481652	10.850644	5.596663
165C_1HR	3.083464	11.394638	11.269687	4.670573
WAITING_1_DAY	4.580573	17.176249	12.115938	9.445539
WAITING_7_DAY	3.855588	19.392548	10.997250	10.560778

4.2 Delta Sigma Analysis on Validation Runs (125C 6 hr. vs 125C 2 hr.)

Based on the evaluation results and the challenges inherent to each condition, optimized settings were selected that minimize processing time without compromising electrical or RF performance.

The challenges are the significant differences in electrical performance, longer processing time, limitation on resources and no existing Moisture Absorption Desorption Study (Appendix A) to be used thus only 125°C 2 hrs. will be considered in the validation runs. Summary is shown in Table 4.

Table 4. Challenges on Different Bake Settings and Waiting Interval Time

Settings	Challenges	Remarks
125°C/10 hours	Longer soaking time Processing time is higher	Not Acceptable
Waiting time 1 day	Significant differences in electrical performance relative to 0 hr	Not Acceptable
Waiting time 7 days	Significant differences in electrical performance relative to 0 hr	Not Acceptable
125°C/1 hour	No moisture adsorption desorption study (Moisture Adsorption Desorption study is required) see Appendix A	Needs MAD study first
165°C/1 hour	Available Jedec trays can handle 150°C maximum Requires device transferring to metal trays	Not Acceptable
125°C/6 hours	Existing longer soaking time Processing time is higher	Not Acceptable
125°C/2 hours	Used in other DFN types (for validation runs to check if significant shifts observed with respect to existing 125°C/6hrs)	Acceptable

Validation runs using bake settings of 125°C 6 hrs. (ref) and 125°C 2 hrs. (2nd pop) coming from the same lot was used. 30 units for each bake setting were used and compared using Distribution Shift Analysis.

Based on two sample proportions, yield is comparable between 125°C 6 hrs. and 125°C 2hrs (see Fig. 8).

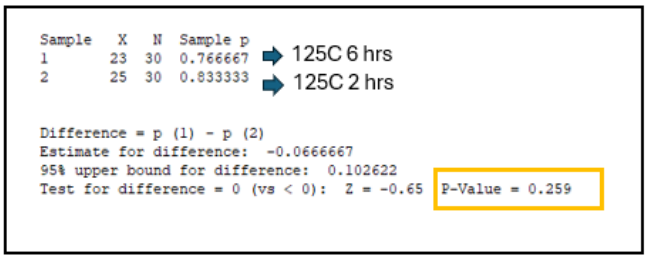

Fig. 8. Two Sample Proportion: Yield Comparison.

On Fig. 9, all parameters passed the sigma ratio criteria, spread is comparable between 125°C 6 hrs. and 125°C 2 hrs.

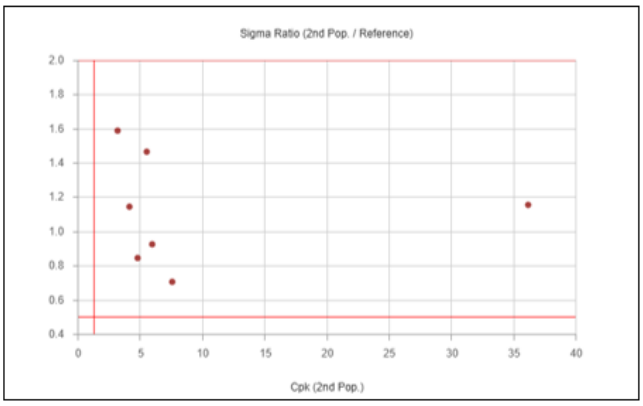

Fig. 9. Sigma Ratio: 125°C 6 hr. and 125°C 2hr.

For median shift, only threshold voltage failed the criteria but with CpK > 1.67 (at 7) , this would not cause any yield loss and will have no issues. See below figure.

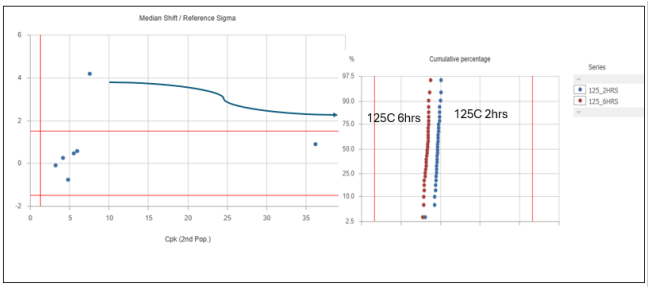

Fig. 10. Median Shift: 125°C 6 hr and 125°C 2hr.

4.3 Recalculation of Processing Time

Using the optimized bake settings of 125°C 2 hrs., 66.7% processing time improvement is observed. Bake settings were aligned with other released DFN package types as seen on Fig. 11.

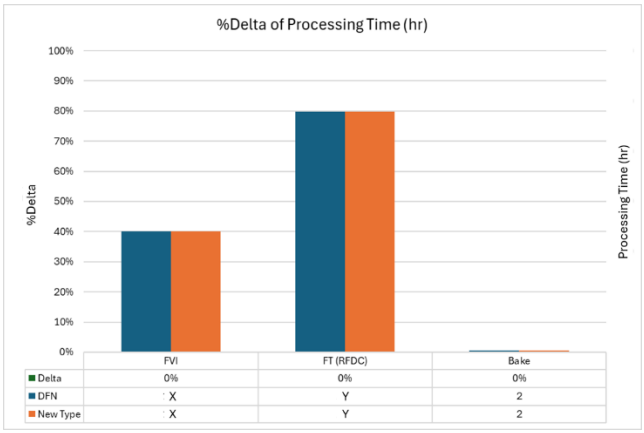

Fig. 11. %Delta of Processing Time per Process after Improvement.

5.0 CONCLUSION

The study evaluated multiple bake settings varying in bake soaking time and temperature, and different waiting time intervals. For each bake condition, electrical and RF performance is also assessed as no significant shifts in RF performance should be observed.

Implementing the optimized bake condition of 125 °C for 2 hours resulted in a 66.7% improvement in processing efficiency, with no compromise to the device's electrical or RF integrity.

6.0 RECOMMENDATIONS

To further explore reduction of processing time, it is recommended to do the Moisture Absorption Desorption study on Bake Settings of 125°C for 1 hr. and evaluate on more lots (different diffusions) to check the trapping related parameters as well in GaN.

7.0 ACKNOWLEDGMENT

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- **Ampleon Shanghai:**
  Judy Li, Danny Du
- **Ampleon Nijmegen:**
- Edwin Orij, Wim Somhorst

8.0 REFERENCES

1. IPC/JEDEC J-STD-033 Bake Conditions, https://www.eesemi.com/baketables.htm

2. SiliconDash® User Guide V36.3

9.0 ABOUT THE AUTHORS

Floralyn Custodio graduated Cum Laude with a degree of Bachelor of Science in Electronics and Communications Engineering from the University of Santo Tomas. She started her career in the semiconductor industry in 2003. She is currently working in Ampleon Philippines Inc. as a Senior Manager in Test Product Engineering Department and mainly handling the development and improvement of different GaN products.

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10.0 APPENDIX

Appendix A. Moisture Absorption Desorption Study

Moisture Absorption Desorption Study

ITEM	DFN Type Lot 1 Mold A	DFN Type Lot 2 Mold A	DFN Type Lot 3 Mold A
maximum moisture absorbed by weight (g) @ MSL3 condition (30 ˚C/60%RH)	0.0022	0.0016	0.0011
time to absorb the maximum moisture (H-hours)	72H	72H	72H
moisture absorb in 12H (g)	0.001	0.0011	0.0003
moisture absorb in 24H (g)	0.0012	0.0012	0.0004
moisture absorb in 48H (g)	0.0015	0.0013	0.0007
moisture absorb in 72H (g)	0.0022	0.0016	0.0011
maximum moisture removed by weight (g) @125 ˚C dry bake	0.0023	0.0017	0.0012
the total time the max moisture absorb can be remove (H - hours)	2H	2H	2H
moisture remove @ 2H dry bake	0.0023	0.0017	0.0012