Trapping Effect Recovery for Gallium Nitride (GaN) Devices

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ABSTRACT

Gallium Nitride (GaN) has emerged as the preferred material in semiconductor technology, offering superior electrical characteristics such as higher breakdown voltage, faster switching speeds, enhanced thermal performance, and lower on-resistance compared to conventional silicon-based devices. As GaN adoption accelerates across various applications, improving process efficiency while maintaining stringent quality standards becomes paramount.

Despite the significant advantages of GaN devices, one of the critical challenges affecting performance is the trapping effect, which can degrade electrical characteristics and reliability.

This study addresses the need to optimize thermal bake recovery processes for next-generation GaN devices where conventional wait times are no longer effective. A Plan-Do-Check-Act (PDCA) approach was implemented to evaluate the impact of bake duration on threshold voltage recovery across different stress sources such as multiple test insertions and burn-in.

Results showed that 1-hour baking at 125°C achieves comparable threshold voltage recovery to a 24-hour bake for test-induced trapping. However, burn-in-induced trapping exhibited poorer recovery and increased Cpk variability under shorter bake durations, especially for specific diffusion lots.

These findings provide a foundation for baking process optimization, contributing to improved test efficiency, reduced cycle time, and sustained quality in GaN device production.

1. 0 INTRODUCTION

In semiconductors today Gallium nitride (GaN) is gaining momentum and now plays a role in multiple market segments, aside from its common use back in the 90's which is generally used in light emitting diodes (LED) used for disk reading [1]. GaN can provide best in class linearity, can operate in high frequency, power efficient and has broadband performance in a relatively small package which makes it more attractive to different market segments.

Despite the outstanding potential and superior performance of GaN devices, one of the challenges is the charge trapping that can limit the dynamic performance of GaN devices [1]

In relation to the known trapping behavior of GaN, assessment is performed to determine the effect on RF and DC test parameters.

The trapping can be manifested in an increased threshold Voltage (Vth), this instability in threshold voltage in relation to trapping was also discussed in detail by M. Chae, H. -Y. Cha and H. Kimin in the journal published by IEEE in which the fundamental mechanisms driving threshold voltage instability in GaN caused by charge trapping is reported[2].

Initial study shows full trapping recovery is not attained after staging the recent generation of GaN in room temperature for 3 days, however full trapping recovery only after 24 hours baking at 125°C as described in Fig. 1.

Extended waiting and 24-hour bake time is not acceptable in mass production manufacturing since it will have a longer processing time and will have a negative impact on the cost structure of the product. It is imperative that the bake time be reduced to be able to deliver quality products at a lower manufacturing cost.

During development, the team has to define the most effective trapping recovery for the new GaN generation subjected to multiple testing and customer specific requirements such as burn in.

The Team made separate assessment for trapping induced by multiple retesting as well as trapping induced by additional burn in.

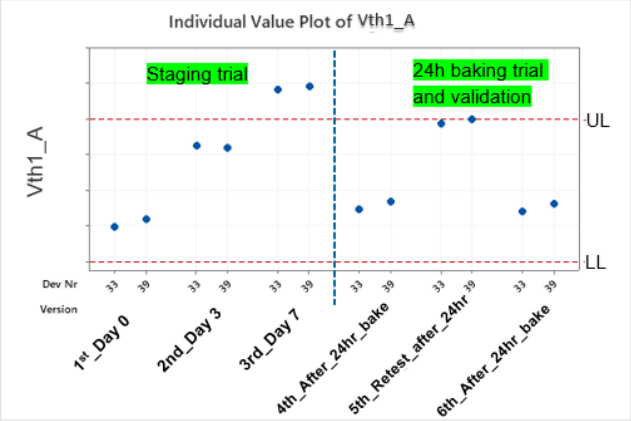

Fig.1. Trapping recovery assessment.

The pilot device involved in this exercise belongs to the recent generation of Doherty GaN device which has 2 sections and is used for S-Band, operating in high frequency and high-power applications.

The result of the study is also applicable on the on-going product development of the same generation and can be used as baseline for the next generation of GaN products.

2. 0 REVIEW OF RELATED WORK

The focus of this study is the charge trapping recovery. Trapping in GaN was explained by M. Meneghini et al in their paper published by IEEE[1] in which it summarizes the most relevant properties of gallium nitride and related transistors, and describes the main challenges related to charge trapping in GaN. Specific attention is given to the dynamic-on resistance process and to the hot-electron trapping phenomena.

In the paper of M. Meneghini et al Two kinds of trapping were discussed the dynamic on-resistance where the transistor is exposed to high off-state bias in which a large voltage difference is applied between gate and drain, and this may lead to the trapping injection. This is particularly interesting for transistor operated in switching-mode power converters, where their bias point is continuously switching from off-state to on-state. This trapping phenomenon can be related to testing in manufacturing set-up.

Another kind of trapping is the Hot-electron effect in which the device is operated in a semi on state where high voltage and a non-zero 2DEG current are present[1], this trapping phenomenon can be relatable to Burn-in which is a customer specific requirement.

Burn-in requirement is becoming an industry standard as we need to ensure the reliability for critical product applications. The purpose of burn-in was further explained by V. Valenta et al. in their paper published by IEEE[2]. It specified that the purpose of burn-in is for the stabilization of active devices after manufacturing to such levels that further drifts are negligible and can be handled by system margins and to screen out unsuitable components for early failure/infant mortality[2].

The paper from M. Meneghini et al describes how the charge trapping was generated and how it impacts the performance of GaN whereas the paper of V. Valenta et al. describes the importance of Burn in. The study that is presented in this paper focuses on the recovery of the new generation GaN devices from this trapping phenomenon induced by testing and burn in to guarantee quality products to our customers.

3.0 METHODOLOGY

This study employed two parallel assessments to evaluate the effectiveness of reduced bake times in recovering threshold voltage shifts caused by: (1) multiple test insertions and (2) burn-in stress. All experiments were performed on recent-generation Doherty GaN S-band devices composed of two sections, both designed for high-frequency, high-power RF applications.

3.1 Methodology for multiple testing trapping recovery

In assessing the trapping recovery for multiple testing, the team was able to evaluate 5 samples and subject that samples to different bake time and multiple testing described in Table 1 using constant temperature at 125°C.

Table 1: Summary of the bake trial

Bake time (Hour)	Test insertion (count)
24	3
8	4
2	4
1	2
0.5	2

3.2 Methodology for burn-in induced trapping recovery

As a customer requirement burn-in will part of the test process. In this case, another assessment has to be done including burn-in in addition to testing.

The assessment was done across 5 lots from 4 different diffusions. Each lot was divided into 4 legs thereby having 250pcs each leg with varying bake times at constant temperature of 125℃ as described in Fig. 2.

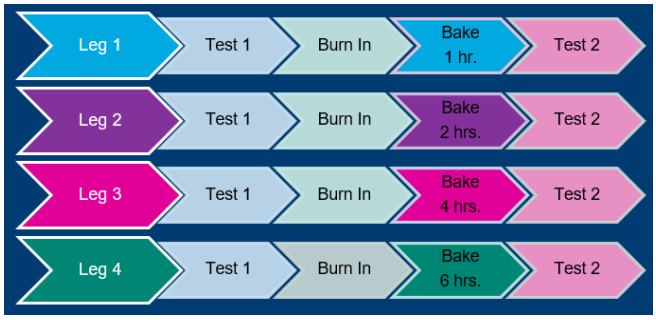

Fig. 2. Different legs for assessment after additional Burn in.

The procedure will include Test 1 to be able to obtain the 0hr data and Test 2 to check the impact of different bake time to recover the 0hr performance.

As described in the related literature, the impact of the trapping can be seen on Threshold voltage. In this regard, the threshold voltage response was analyzed to be able to establish the bake time for trapping recovery.

4.0 RESULTS AND DISCUSSION

The results of each methodology were analyzed with respect to threshold voltage, as this parameter is known to be influenced by charge trapping effects, as documented in related literature

4.1 Multiple test trapping recovery results

The Threshold Voltage parameters were observed in each of the runs. Different bake times were compared and assessed. It shows an Increasing trend with ~30mV as bake time is reduced. However, immediate retest shows reduction of ~650mV regardless of bake time as illustrated on Fig 3. Assessment shows that 1hr baking has minimal differences between 24hr and 1hr baking.

4.2 Burn-In recovery and Statistical Impact

As mentioned during methodology, 4 legs were subjected to different bake time. Results were analyzed with respect to threshold voltage and median value for each leg was plotted as shown on Fig. 4. Test 1 indicated in the legend is the 0hr data and Test 2 will represent the results after baking, the aim is to recover the readings to the level of 0hr.

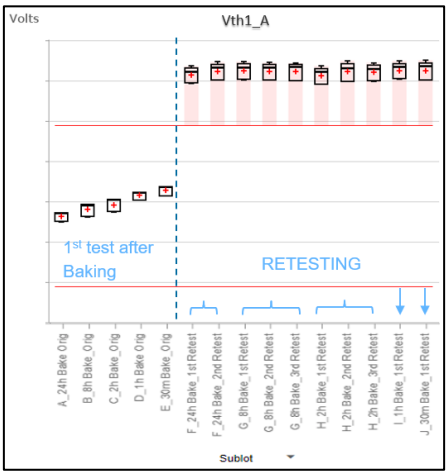

Fig 3. Vgs1 response in different bake time and test insertions.

It shows that the threshold voltage is higher at lower bake time thereby increasing the delta with respect to 0hr. This increase in median values becomes more critical as it approaches the upper specification limits.

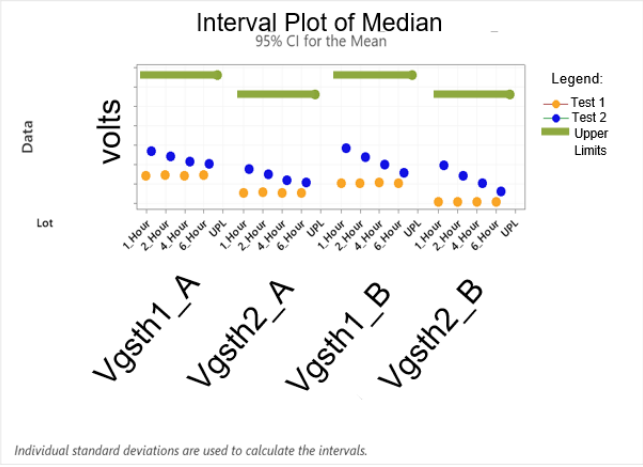

Fig 4. Interval plot of Threshold Voltage Median per leg.

In addition, the Cpk of threshold voltage was also observed to consistently fall below 1.67 for both 1-hour and 2-hour bake times (highlighted in red circles) on Fig. 5.

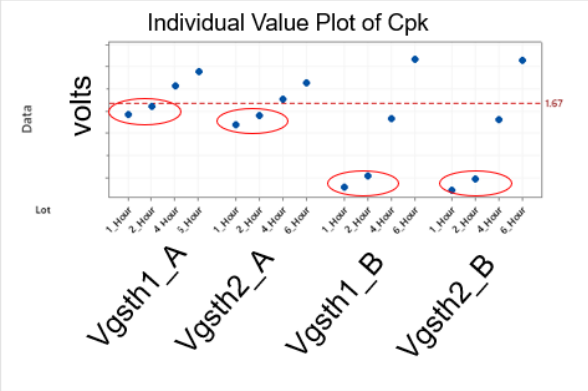

Fig. 5. Cpk of threshold voltage per leg.

This suboptimal Cpk is primarily due to an increased standard deviation caused by an outlier lot (indicated by red boxes) on Fig. 6 where it is also observed that this low Cpk is attributed to section B in blue box.

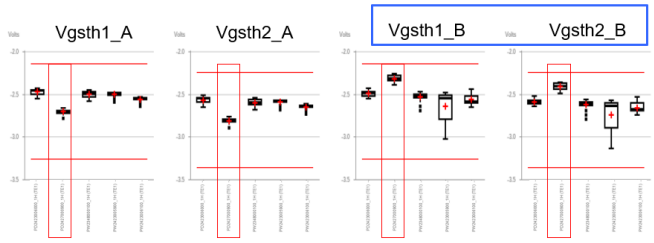

Fig. 6. Box plot of 5 lots included in 1-hour bake time leg.

Since the poor recovery and low cpk is attributed to 1 lot, the team look into the threshold voltage diffusion performance. It can be seen on Fig. 7 the wafer test data of the product. The diffusions utilized for this trial are highlighted and the diffusion of the lot with a low Cpk at the final test is indicated by the red box.

The threshold voltage spread of the diffusion used in the trial lots are bounded by the blue lines and marked by the orange box are the threshold values that was not fully covered in the trials. This incomplete coverage of diffusion performance may result in yield loss at 1-hour and 2-hour bake times due to poor Cpk.

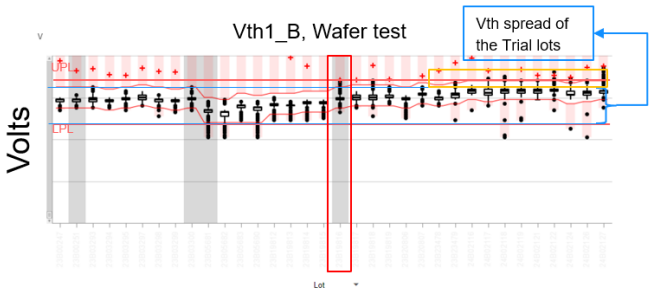

Fig 7. Wafer test performance of the trial lots.

The impact of bake time on trapping parameters reveals a clear relationship between shorter bake durations and decreased process stability of Threshold voltage. A lower bake time has increased Threshold voltage seen on Test 2, which directly contributes to a reduction in Cpk values.

Throughout trials, the Cpk values remained consistently below 1.67 for both 1-hour and 2-hour bake times, indicating a significant deviation from optimal yield expectations. A diffusion analysis suggests that the primary factor behind these low Cpk values is diffusion-related differences. Furthermore, the threshold voltage spread of the diffusion within the trials does not sufficiently cover the performance across all the available diffusion potentially causing yield loss at both 1-hour and 2-hour bake durations due to poor Cpk performance.

After assessment of different bake time on parameters affected by trapping which is inherent on GaN devices. The study findings suggest that one (1) hour bake time shows acceptable results for multiple testing trapping recovery and four (4) hours bake time can be utilized to recover trapping induced by burn-in without substantially impacting Cpk values using constant temperature of 125°C.

5.0 CONCLUSION

The study findings indicate that trapping recovery characteristics vary across different generations of GaN technology. For earlier GaN generations, a waiting period for trapping recovery proves effective; however, this approach is not applicable to the latest GaN generation, where alternative recovery mechanisms may be required.

Additionally, any process step involving gate bias—such as electrical testing and burn-in—introduces additional charge trapping effects, which requires a thorough assessment of the corresponding trapping recovery dynamics. Experimental results demonstrate that a one (1) hour bake at 125°C yields acceptable retest recovery performance for trapping effects

induced by standard electrical testing, whereas a four (4) hour bake at 125°C is required to mitigate trapping induced by burn-in stress conditions.

These findings serve as a foundational reference for optimizing trapping recovery strategies in next-generation GaN technologies, particularly as GaN continues to gain traction in various market segments, including consumer electronics, automotive applications, telecommunications, and healthcare[4]. Further investigations will be necessary to refine recovery protocols for emerging GaN architectures to ensure reliability and performance consistency.

6.0 RECOMMENDATIONS

The team recommends a systematic evaluation of trapping recovery mechanisms across different GaN generations to account for variations in charge trapping behavior and reliability performance.

Furthermore, a comprehensive assessment of the recovery methodology is advised for each process step that involves application of gate bias, as well as thermal exposure conditions.

Establishing a standardized recovery approach tailored to specific GaN architectures will be critical for maintaining performance consistency and yield optimization in advanced semiconductor applications.

7.0 ACKNOWLEDGMENT

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8.0 REFERENCES

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9.0 ABOUT THE AUTHORS

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10.0 APPENDIX

This section is not applicable.