Test Time Reduction Through Six Sigma Methodology, an Enabler for High Volume Manufacturing

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ABSTRACT

In the manufacturing industry, maximizing profit is essential to enable reinvestment in emerging technologies such as Artificial Intelligence (AI). Achieving this requires highly efficient processes. This principle is particularly critical in high-volume semiconductor manufacturing, where minimizing the Cost of Goods Manufactured (COGM) directly enhances product margins.

To address this, a dedicated team was formed to identify and implement COGM reduction strategies. One key focus area was the reduction of test time, as testing duration is often directly proportional to cost. This paper presents a Lean Six Sigma approach to test time reduction using the DMAIC (Define, Measure, Analyze, Improve, Control) methodology, a widely adopted problem-solving framework in the industry.

In the Define phase, a pilot product was selected for analysis. During the Measure phase, potential contributors to extended test time were identified and validated. The Analyze phase pinpointed the primary factors impacting test duration. These factors were addressed in the Improve phase, where solutions were implemented across multiple devices. Finally, in the Control phase, documentation and processes were updated to ensure sustained improvements.

As a result, test time was reduced beyond the initial target, yielding a cost savings of USD 28,000. The methodology demonstrated here is adaptable and can be applied to process optimization initiatives across various manufacturing domains.

1. 0 INTRODUCTION

Test Process is one of the few imperative things to ensure quality produce across industries. Test improvement being a key factor in effective manufacturing, most specifically in the semiconductor industry to ensure quality and yet cater with the highest possible output.

Test time is a crucial factor to improve, especially in the test program development maturation, as it directly affects the efficiency and productivity of the test process. Reducing test time significantly lowers costs and accelerates the release of high-quality test program offering competitive edge.

Subsequently, during the start of 2023, a company target; to lower the cost of goods manufactured (COGM) triggered a roll out for test time improvement of high-volume devices. However, achieving substantial reductions in test time is challenging due to the complexity of unmapped software systems and the need for comprehensive evaluation.

In this paper, the DMAIC approach driven by six sigma methodology is used to identify the test case with the highest execution time impact and potential for optimization, thereby reducing overall test time without compromising test coverage.

2. 0 REVIEW OF RELATED WORK

Studies made by Jen-Chieh Yeh et.al.[1], proposed a systematic approach to reduce DRAM test time through compaction methods, achieving a 19.5% reduction. These include redundant test item removal, test merging, and creation of efficient patterns. While effective, these methods required long development cycles.

On the other hand, this paper had to accelerate reduced test time to support high-throughput production. Moreover, in this study, tests were streamlined for the reduction of sweep steps and removal of non-datasheet parameters, which are the items explored to expedite implementation without sacrificing our test detectability.

3.0 METHODOLOGY

This project utilized the DMAIC Six Sigma methodology, as it is one of the most effective approaches for project improvement and problem solving. Using the Roos Cassini as the high-performance test platform for the RF LDMOS devices, a significant reduction of parameters and test settings improvement were achieved. The different phases will be discussed below.

3.1 Define Phase

Part of the Cost of Goods Manufactured (COGM) is the reduction of test time for high-volume runner devices. The test time defined in this project is the time incurred from the start of first parameter up to the last test parameter on pass devices only, this is best described in Fig. 1.

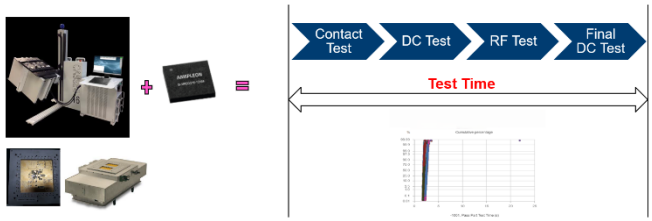

Fig. 1. Test Time Description.

The target device in this project had significant production volume in 2023 and with the highest test time based on 2022 actual average pass part test time indicated by red box on Fig. 2. This project aims to achieve a 30% reduction in test time for the identified pilot device.

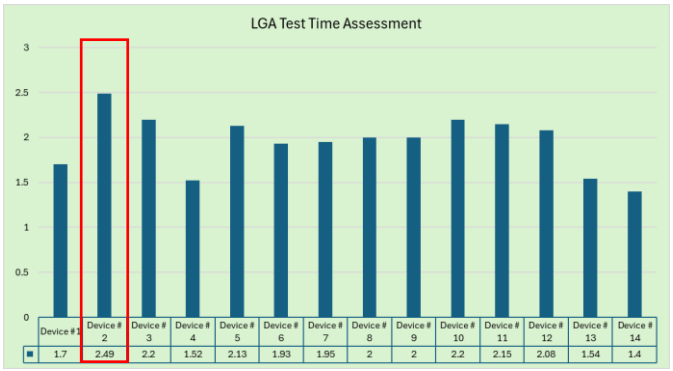

Fig.2. 2022 Test time assessment across devices using the same package outline.

3.2 Measure Phase

In this phase, the project identified which test contributes the most to the overall test time and can be improved in the test program. The team was able to identify the test parameter with the highest contribution through the test time profile as seen on Fig. 3.

Using the cause-and-effect matrix, potential causes and their priorities were defined, as each is characterized by a different type of input. Factors identified include tester hardware update, alignment of the Test program parameters with the customer datasheet and reduction of the test program's sweeps and settling time. Additionally, the test program should not contain any redundant parameters.

The method adapted to improve these factors ensures that we can still guarantee functionality according to customer specifications, and that testing is conducted in the most efficient way possible.

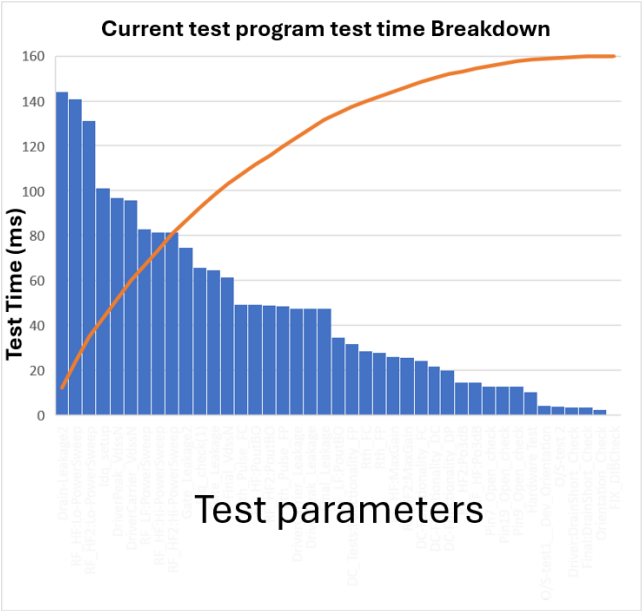

Fig. 3. Test Time profile which shows the contribution per parameter

The update of the tester hardware was identified as one of the factors as there is a significant difference in the test time per tester as shown in Fig. 4, based on the analysis this is attributed to the difference in CPU speed per tester, the update of the CPU speed was deemed necessary and become part of quick wins.

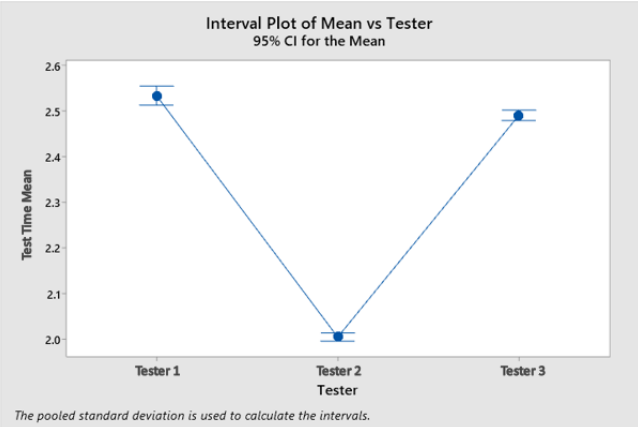

Fig. 4. Interval plot of test time means vs tester

Each major block of the test program was further broken into different test sections shown on Fig. 5. The corresponding test section containing the test parameter with the highest test time contribution will be prioritized for improvement.

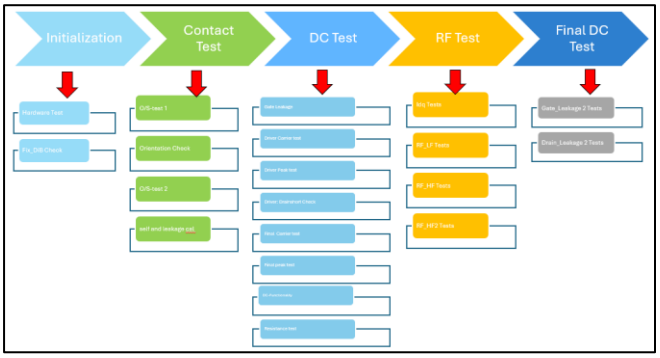

Fig. 5. Test program process flow diagram.

3.3 Analyze Phase

A review of the parameters with the highest test time identified six potential critical factors that could impact test time efficiency. Each factor was evaluated based on practical theories, validity, and estimated impact on test metric as shown in the Table 1.

The sample validation on the removal of monitoring parameter is presented on Fig. 6. where 24 samples were tested using the old and the new improved test program. With a p-value of 0, rejecting the null hypothesis means that the removal of monitoring parameters has significant effect in test time reduction.

To ensure that the removal of monitoring parameters does not compromise the quality of the test program screening, a good correlation analysis should be achieved. This means that the remaining parameters still correlate well with the original full set and still capture the essential behavior or trends. In Fig. 7, it can be seen that perfect correlation is achieved on the removed parameter versus the remaining parameter using different frequency.

Table 1. Table of potential factors with impact on test time

No.	Process	Potential Critical X's	Practical Theory	Decision (Valid/Not Valid)	Test for Significant P-value	Significant / Not Significant
1	FT	Monitoring parameters used by development still in place	There are non-datasheet parameters on the test plan	Valid	0	Significant
2	FT	The test set of new devices are not the same as the test set of old devices	Learnings from new types not implemented on old types	Valid	0	Significant
3	FT	Power sweep resolution that will give acceptable MSC results not defined	Not reduced power sweeps	Valid	0	Significant
4	FT	Frequency sweep resolution that will give acceptable MSC results not defined	Not reduced frequency sweeps	No Data	N/A	N/A
5	FT	Settling time that will give acceptable MSC results not defined	Not reduced settling time	No Data	N/A	N/A
6	FT	Correlated parameters that have the same coverage not removed	No correlation study for similar parameters	Valid	0	Significant

After validating six potential critical factors affecting test time, four were found to have a significant impact. These include: (1) the continued use of monitoring parameters from the development phase, which are no longer necessary in production; (2) discrepancies between test sets for new and legacy devices, which were confirmed to have a minor but valid impact; (3) the absence of optimized power sweep settings; and (4) the presence of redundant test parameters lacking correlation studies, which contributed substantially to increased test duration.

Items	Details
Practical Problem	Is there a difference in test time between old test plan and new test plan in terms of monitoring parameters?
Null Hypothesis	Ho: $\mu_{old-new} = 0$
Alternative Hypothesis	Ha: $\mu_{old-new} \neq 0$
P-Value	0.000 (Reject Ho)
Practical Conclusion	Removal of monitoring parameters have significant effect on test time reduction.

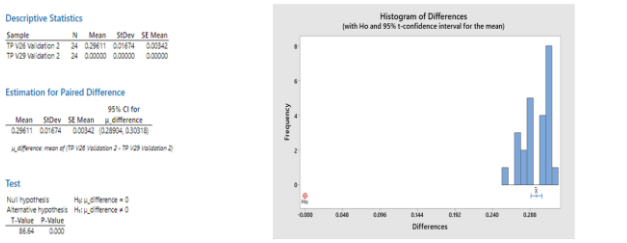

Fig. 6. Sample validation plan for the removal of monitoring parameters.

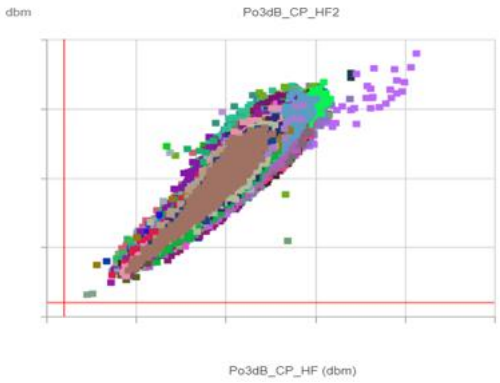

Fig. 7. Correlation analysis on Po3dB using different Frequencies

4.0 RESULTS AND DISCUSSION

As a result, several key items were identified for the test time reduction that need improvement. These include: (1) removal of monitoring parameters, (2) standardization of test settings, (3) reduction of power sweep, and (4) removal of correlation parameters.

These actions led to significant reduction in test time. From 2057ms to 1478ms for 24 samples as shown in Fig. 8.

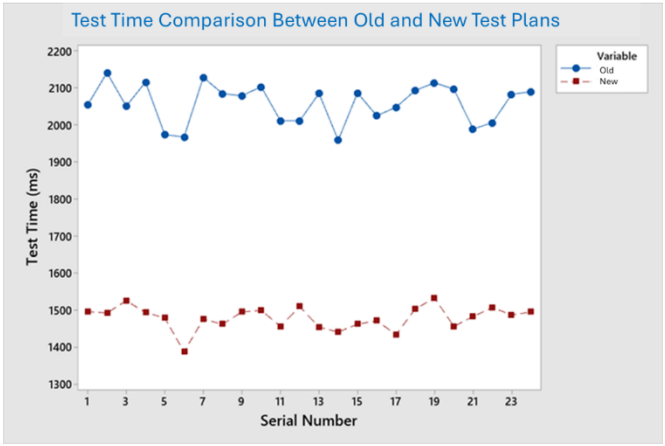

Fig. 8. New test plan/program showing significant test time reduction

With a very favorable initial result, the new test program was implemented in production. Fig. 9 showed a significant test time reduction on the volume runner device.

Due to the success of the initial device, the test time reduction project was also implemented to other 3 volume runner devices. Fig. 10 showed significant test time reduction on all devices. The effort was widely recognized in the company, bringing the much-needed COGM savings.

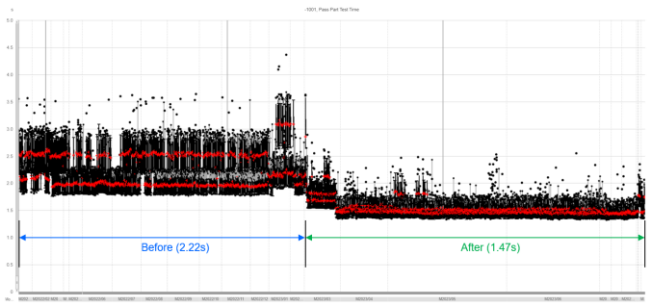

Fig. 9. Test time reduction realized in volume runner device

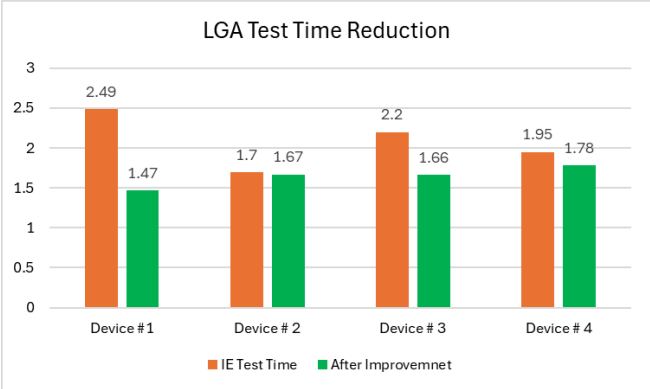

Fig.10. Test Time Reduction on 4 Devices using the same package

Fig. 11 is the summary of Critical X's and can be used as future value stream mapping (VSM) for all incoming new devices, as well as released devices that have significant volume.

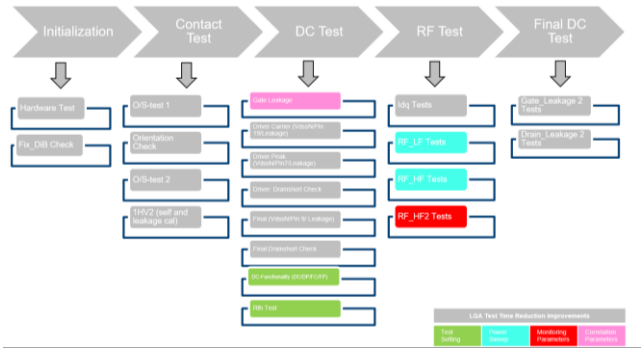

Fig. 11. Future VSM for similar devices tested in Roos

5.0 CONCLUSION

By implementing the Six Sigma methodology, the requirements of High-Volume Manufacturing (HVM) can be provided through the Test Time Reduction (TTR), achieved without compromising product quality or altering the product's form, fit and function.

As a result, processing time per 100,000 units was greatly reduced from 128 to 95 hours, translating to $28,000 cost savings. This efficiency gain enhances on-time delivery performance, thereby improving overall customer satisfaction.

6.0 RECOMMENDATIONS

It is recommended to standardize the implementation of Test Time Reduction (TTR) initiatives across all High-Volume Manufacturing (HVM) devices using Six Sigma methodologies, as a strategic component of the company-wide Cost of Goods Manufactured (COGM) optimization program.

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8.0 REFERENCES

1. Jen-Chieh Yeh, Shyr-Fen Kuo, Cheng-Wen Wu, Chih-Tsun Huang and Chao-Hsun Chen, "A systematic approach to reducing semiconductor memory test time in mass production," *2005 IEEE International Workshop on Memory Technology, Design, and Testing (MTDT'05)*, Taipei, Taiwan, 2005, pp. 97-102.

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