Achieving ±0.5% Current Sense Accuracy in NexFET™ Based Power FET Devices

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ABSTRACT

Current Sense (CS) circuits are widely used in e-fuse devices to accurately monitor system static and dynamic power consumption. In Texas Instruments an e-fuse device which uses NexFET™ based power FET current is sense internally through the IMON(current monitor) pin. These devices are tested in sockets during production, but in real customer applications, they are soldered directly to PCBs. This difference leads to variations in the measured current sense values due to changes in contact resistance, which can be affected by socket pin wear and tear, pressure differences, and mechanical alignment issues. As a result, the current distribution in the socket can become uneven, leading to inaccurate trimming and a mismatch between test and actual performance. The current production test setup has a Machine Guard Band (MGB) of 0.7% and a design accuracy of 2.3%, leading to a total IMON accuracy of about 3%. This paper discusses the impact of socket-related variations on current sensing and outlines a method to reduce CS variation during testing. The goal is to improve accuracy in the production environment, reducing the IMON error from ±3% to ±2.5%, thus achieving better accuracy.

1. 0 INTRODUCTION

In production, Texas Instruments devices are being trimmed and tested using socket/contactor (Figure 1.). On the customer side, however, these same devices are soldered directly onto PCBs (Figure 2.). This difference in setup can lead to variation in current sense (CS) readings. In general, devices that are soldered down show more accurate and consistent current sensing compared to those tested in sockets.

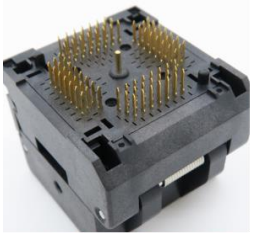


Figure 1. Test Environment

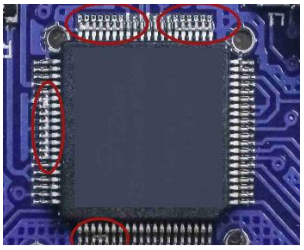


Figure 2. Customer Application

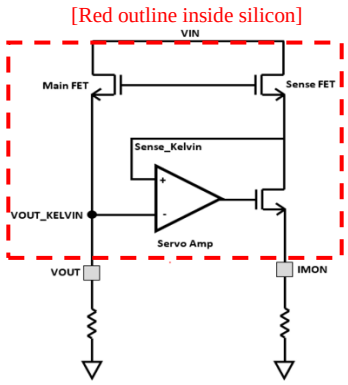
This is a quality risk since the variation can be quite high. What we guaranteed in production can be different from what we see in customer side. Current flow through solder is more uniform. However while kept in socket, current distribution changes as contact resistance changes.

Contact resistance varies due to worn out pins, planarity issues and pressure variation in handler. This causes wrong trimming and large delta with respect to solder (customer board) causing quality risk.

In socket, different socket pins will have different resistances. Hence current distribution is majorly controlled by these resistances. If socket set-up is bad, the current sensing magnitude of device will be trimmed to adjust to unequal distribution of current through the device. Once kept in a uniform distribution set-up (customer board), the current sensed will be different. This shows up in socket to solder variation.

The impact of this variation also depends on how the current sense architecture is implemented, particularly the placement of the sense points. Devices with sense points closer to regions affected by contact resistance are more likely to show significant deviation. Reducing this variation during testing is important to ensure CS accuracy aligns with real-world performance.

1.1 Current Sense Circuit



In Figure 3. The sense ratio (KSNS) is evaluated as the ratio of Main FET & sense FET currents

KSNS = IMainFET / IsenseFET

By Ohm's Law as long as voltage stays the same if resistance increases current decreases and vice versa that's why contact resistance variation in socketed test setups can significantly impact the current sense ratio in e-Fuse devices, which rely on accurate matching between load current at VOUT and sense output at IMON. Unlike soldered connections that offer stable, low-resistance paths, socket interfaces introduce variable resistance due to pogo pin wear and tear, uneven contact force, contamination, or mechanical misalignment. These variations lead to non-uniform current distribution across the power and sense paths, affecting the internal balance between the power FET and sense FET. As a result, the device may be improperly trimmed during test, causing the sensed current to deviate from actual values once deployed in soldered customer applications. Minimizing contact resistance variation is therefore critical to ensure consistent current sense accuracy between production and end-user conditions.

2. 0 REVIEW OF RELATED WORK

Refer to 1.0 Introduction.

3.0 METHODOLOGY

3.1 Materials

The following are the materials and software needed to determine the lowest VOUT skew case for TI eFuse device (DOE) with minimum number of ballasting resistors.

- Third-party simulator
- Third-party PCB designer software
- TI eFuse device
- Load Board
- Final Test device tester

3.2 Procedure

3.2.1 For VOUT Sense point selection method:

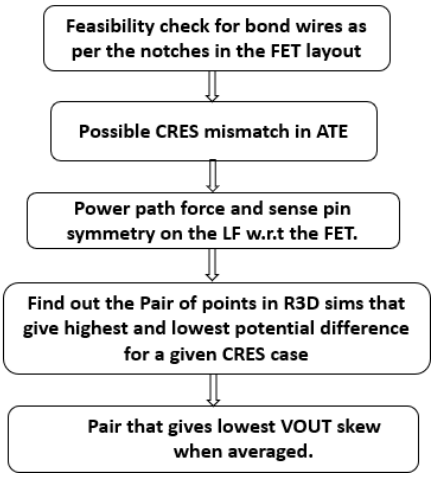


Figure 4. VOUT Sense Point Selection Method

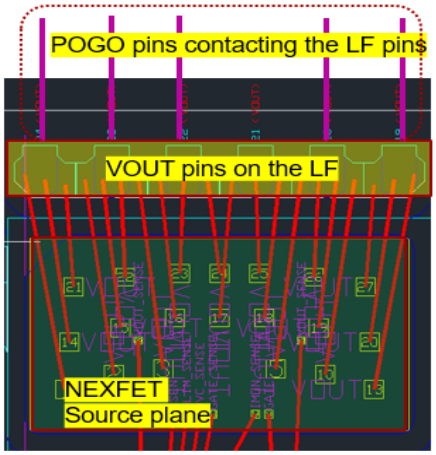


Figure 5. NexFET™ VOUT pad placement + bond wires + LF pins + Pogo Pins

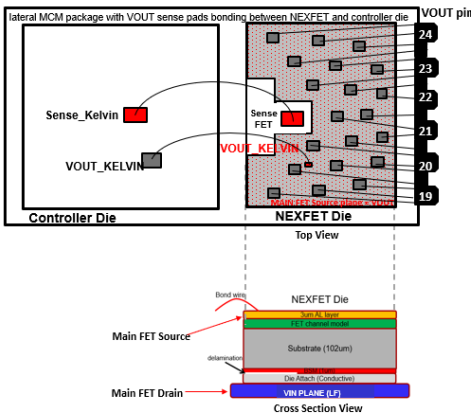


Figure 6. Top and Cross Sectional view of MCM Chip

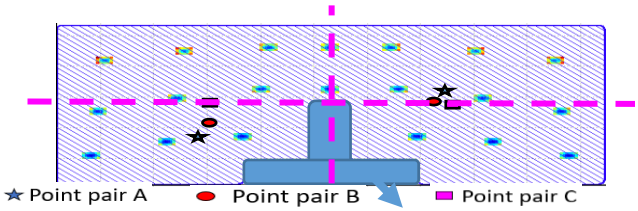


Figure 7. Notch with Sense FETs and Bondpads.

VOUT skew = [VDS(main FET) – VDS(sense)]/ VDS(main FET) *100

For single point Vout sensing, Vds is straight forward. Vds(sense FET) = Vd -Vs

The gradient represents the potential difference. It is biggest where the potential contour lines are closest and is minimal where the potential contour lines are spaced apart.

Baseline case is best case scenario with all POGO pins connected to LF pins 24-22, 20-19 and no CRES variation issue seen on pins.

Table 1. Comparison of VOUT skew for different CRES cases with existing solution(NO averaging) and proposed solution(with 2 point averaging)

		VOUT skew in %							
Current Solution		case1F(baseline)	case2F	case3F	case4F	case5F	case6F	case7F	case8F
		0.581	6.027	0.298	4.090	0.683	4.541	5.417	4.859
Proposed Solution	Point Pair A	0.565	0.173	0.555	0.438	0.418	0.665	0.933	0.793
	Point Pair B	0.392	0.134	0.517	0.200	0.324	0.507	0.894	0.679
	Point Pair C	1.373	1.176	1.219	1.344	1.368	1.560	1.270	1.424

For 2 point VOUT sensing(proposed solution), VOUT at sense point 1, sense point 2 is measured and Vds(sense)= Vd –[Avg(VOUT1, VOUT2)].

Based from the above table (Table 1) current solution(no sense averaging) approach case3F has the least VOUT skew while the proposed solution(with 2 point averaging) at three different point pair combinations, Point Pair B has the least VOUT skew in all CRES cases.

By having one more sense point will give more accurate VOUT information when VOUT potential is skewed but sense points must be bondable. Hence must not coincide with 20 VOUT bondpad locations or cause ARC violations with the respective bondwires.

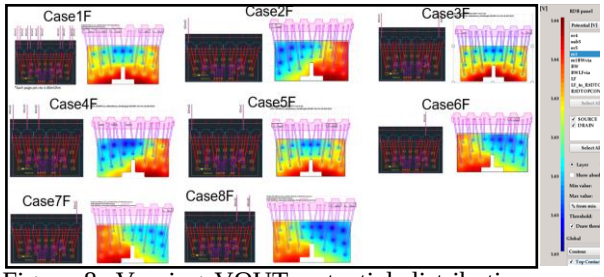


Figure 8. Varying VOUT potential distribution across the NexFET™ for different POGO pin connections due to changing CRES .

CRES(accumulated resistances of Final Test hardwares and device) variation on the POGO pins impacts the VOUT potential distribution on the NexFET™ `s source plane and thereby affecting the current distribution as shown in Figure 8. It also shows that single point VOUT sensing will not be accurate due to CRES variation.

3.2.2 Optimum Ballasting Configuration.

We need to do CRES simulation using the third-party simulator to account and to avoid socket to solder differences affecting current sense accuracy. During Final Test, the device is not soldered to the test board and pogo pins are used for contacting the device pins instead. The contact resistance of these pogo pins serve as current sources for the device pins. If contact resistance variation is not considered, then it will lead to inaccurate trimming of sense FET. This device when used on customer board will not be effective during CS functionality. Different cases of CRES variation must be modelled along with the bondwire resistances and current distribution across the FET must be analyzed + ballasting resistor(Rballast). Rballast ensures contact resistance variation wont impact current distribution. Requires extra board resistors with high power rating. Optimum ballasting configuration refers to least number of ballast resistor used with the lowest VOUT skew. VOUT must be sensed at 2 points on the FET which give the average VOUT potential for all cases of CRES, temperature, potential variation.

Below are the simulation result of different cases.

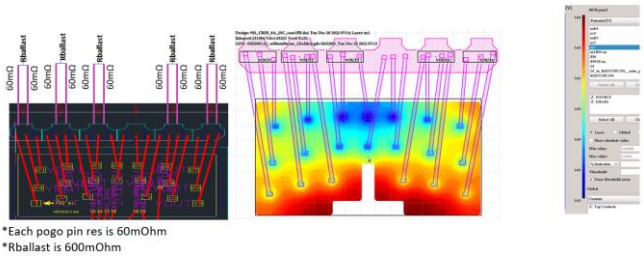


Figure 9. Case1FB (Baseline case) : 10 pin connector with 2 pogo pins each on pin# 24-22, 20-19, no pogo pin on pin #21; 8A; 25C ; Lead Frame is fused, Ballasting

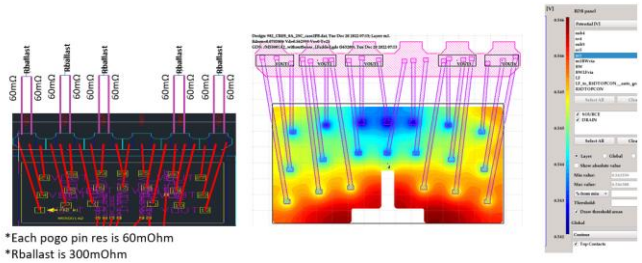


Figure 10. Case2FB (Baseline case) : 10 pin connector with 2 pogo pins each on pin# 24-22, 20-19, no pogo pin on pin #21; 8A; 25C ; Lead Frame is fused, Ballasting

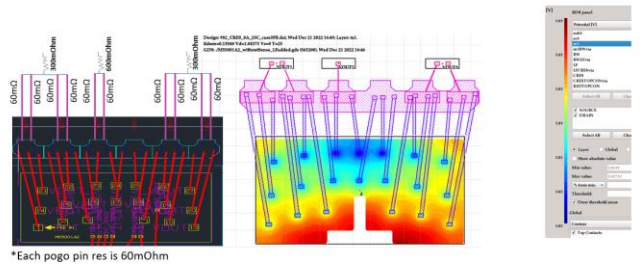


Figure 11. Case3FB : 3 ballasting resistors with 2 pogo pins each on pin# 24-22, 20-19, no pogo pin on pin #21; 8A; 25C ; Lead Frame is fused, Ballasting(Target: least number of Rballast, lowest possible value of Rballast)

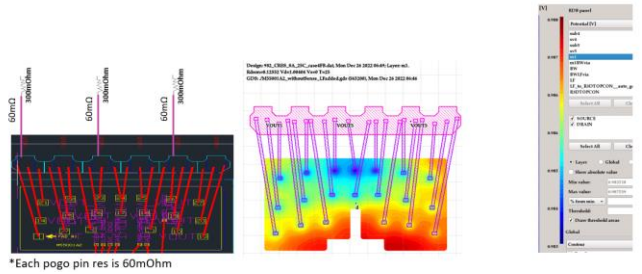


Figure 12. Case4FB : 3 *300mOhm ballasting resistors with 1 pogo pin each on pin# 24,22,20; 8A; 25C ; Lead Frame is fused, Ballasting; (Target: least number of Rballast, lowest possible value of Rballast)

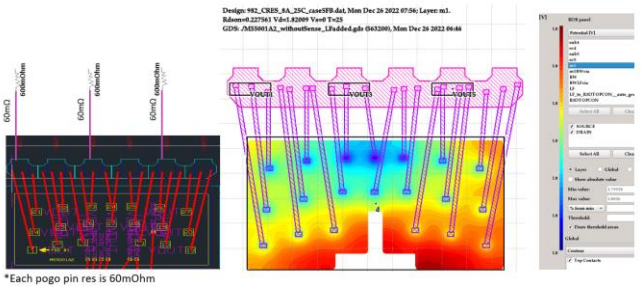


Figure 13. Case5FB : 3 * 600mOhm ballasting resistors with 1 pogo pin each on pin# 24,22,20; 8A; 25C ; Lead Frame is fused, Ballasting; (Target: least number of Rballast, lowest possible value of Rballast)

Table 3. VOUT skew result of Optimum Ballasting Configuration.

Single (982)	Fused LF											
	case1F(baseline)	case2F	case3F	case4F	case5F	case6F	case7F	case8F	case1FB	case2FB	case3FB	case4FB	case5FB
	0.581	6.027	0.298	4.090	0.683	-4.541	-5.417	-4.859	0.604	0.585	0.590	1.127	1.105327001

Based from the above data case3FB is the optimum ballasting configuration, having 3 ballasts resistors. 300mOhm Rballast at pins 19&20, 600mOhm Rballast at pin22 and 300mOhm at pins 23&24 respectively.

Below is the actual schematic implementation of ballasting resistors.

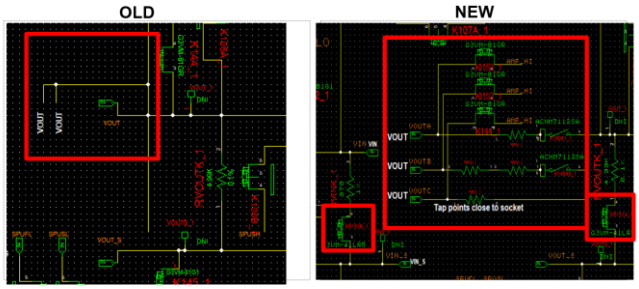


Figure 14. Old HIB Schematic(w/o Rballast) VS New HIB Schematic(w/ Rballasts)

From a single point VOUT(Old HIB), new HIB design has 3 VOUTs each having a ballast resistor.

4.0 RESULTS AND DISCUSSION

In existing solution, test Machine Guard Band(MGB) is 0.7% and with design accuracy of 2.3%, total IMON accuracy is 3%.

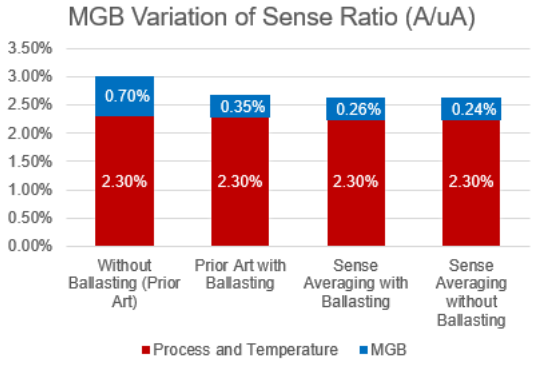


Figure 15. MGB Variation of Sense Ratio (A/uA)

From the above figure (Figure 15.) we can see MGB improvement from 0.7% to 0.35% with ballasting only, to

0.26% with VOUT Sense averaging and ballasting, to 0.24% with VOUT Sense averaging only which translates to Final Test yield improvement and productivity improvement since lot on hold due to this yield issue was minimized.

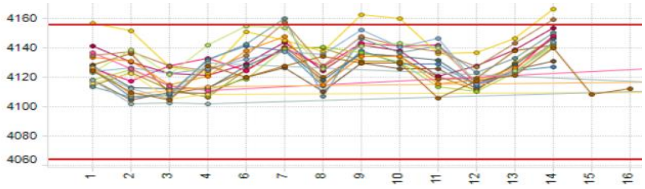


Figure 16. Prior Art

Without any sense averaging, Figure 16 shows a significant Final test yield loss of around 5% for Sense Ratio.

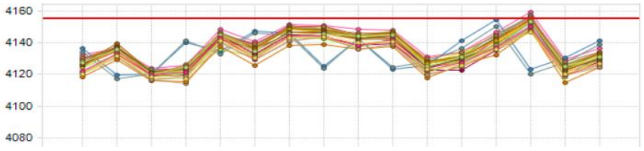


Figure 17. Proposed Test Sol'n: Existing sol'n + ballasting

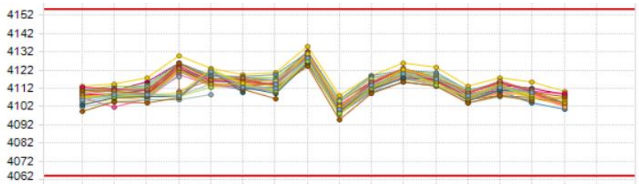


Figure 18. Proposed Design Sol'n: Sense Averaging

With sense averaging and ballasting, Figure 18 shows lesser yield loss for Sense Ratio.

5.0 CONCLUSION

Both the proposed solutions are showing similar results. IMON accuracy has been improved from 3% to 2.5% because of reduction in MGB from 0.75% to <0.24%. Final Test Yield Loss was reduced from 5% to 0.2% at the production site thus minimized the hold lots due to this yield issue. Number of insertions for high running silicon will be reduced to one (FT2 will be removed) and thus causing a decrease in Test Cost by 25%.

6.0 RECOMMENDATIONS

DFT(Design For Test) solution is showing similar results as Design Enhancement . However DFT solutions requires tremendous amount of simulations in VOUT Sense averaging and an extra hardware cost added for Ballast resistors. Authors recommendation is to focus on Design Enhancement.

7.0 ACKNOWLEDGMENT

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8.0 REFERENCES

1. CRes_Training.ppt
   By: Michelle Uy Siaotong, May 16, 2006

2. De-Sensitizing Current Sense Ratio Measurement Accuracy from Contact Resistance in ATE.ppt
   By: Gaurav Mittal, APP PSIL_PS Test Team, 2021

9.0 ABOUT THE AUTHORS

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10.0 APPENDIX

This section includes figures and tables that are too bulky to be placed next to the discussion. It helps to maintain the smooth flow of discussion while maintaining the technical merit of the study through appropriate data and figures. Each appendix should be identified using an alphabet, with corresponding description (e.g., Appendix A – Cumulative Standard Normal Distribution Constants).

Other Pointers:

One should refrain from beginning a sentence with numbers or acronyms.

The first time an acronym is used in the text, it should be defined. When the paper has lots of acronyms in use, a list of definitions in a separate section can be created.

Text should be written in third person passive mood. Refrain from the use of personal pronouns.

Check to see if your figures have labels which are readable. The figure should be able to convey the message without one's having to read the text of the manuscript. Hence, the figure captions should be able to explain the figure.

Do not be redundant with your data presentation, some people have the tendency to show the tabular data form as well as the chart. Whenever possible, charts and graphs are preferred over tabulations of data points.

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