STRIP CONVERSION KEY STRATEGIES & INNOVATIONS FOR A FAST TURNAROUND IN CLARK QFN

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ABSTRACT

Manufacturing cycle time, test setup requirement, setup conversion time, and overall test cost are ultimately high using pick-and-place (PnP) flow. In 2022 Final Test is struggling to hit the daily run rate given that half of Clark volume was processed via PnP flow, while remaining volume was on strip flow. The team's goal is to achieve complete strip volume penetration in a three-year time frame and in order to achieve this goal, all Pick and Place devices need to be converted to strip flow.

In this paper, the team will discuss three key strategies; which merely evolved on (1) design and full conversion to roadmap test solution, (2) leverage strip solution from TI A/T sites, and (3) cost-efficient innovations: PnP to strip interposer solution and strip-to-strip hybrid contactor. Penetrating Strip Volume through strategic conversion brought line stability, space and set-up requirement savings which resulted to Improved Cycle Time, Cost Savings and produced more Outs.

These strategies enable the team to transition to strip form testing wherein it achieved improve throughput by testing multiple units simultaneously, reduce handling time and cost per unit, especially for small form-factor devices, enhance automation across the back-end process, minimizing manual intervention, support high-volume production with scalable and streamlined workflows. This strategic move positions us to better serve customer needs, improve operational efficiency, and stay competitive as packaging technology continues to shrink and diversify.

1. 0 INTRODUCTION

Semiconductor processing is the complex and highly precise series of steps used to manufacture semiconductor devices, which are the fundamental building blocks of modern electronics. These devices, such as transistors, diodes, and integrated circuits (ICs), are fabricated primarily on silicon wafers through a sequence of physical and chemical processes.

The process begins with the preparation of ultra-pure silicon wafers. Once wafer is ready for assembly, it goes to the processes which includes wafer dicing, die attach, wire bonding, molding, symbolization, singulation, final testing, then tape and reel process as shown in Fig. 1.

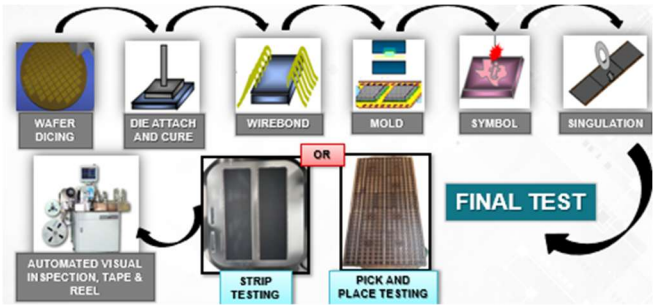

Fig.1 Semiconductor manufacturing process flow.

Final testing is the last critical step in the semiconductor manufacturing process, where each completed chip or device is thoroughly tested to ensure it meets all functional, performance, and reliability specifications before being delivered to customers.

After packaging, semiconductor devices undergo electrical testing using automated test equipment (ATE). These systems apply input signals and measure the output responses to verify that the chip operates correctly under various conditions, such as different voltages, temperatures, and signal frequencies.

In the Final Test stage of semiconductor production, packaged devices must be tested for functionality and performance. Two common approaches for handling and testing these devices are Pick-and-Place (PnP) and Strip Form Testing. Each method has advantages and is suited to different types of products and production goals.

1.1 Pick-and-Place (PNP) vs Strip Form Testing

Pick-and-Place (PNP) testing is where an individual packaged device is picked from a tray or tube and placed into a test socket on the Automated Test Equipment (ATE). After testing, the devices are sorted (good vs. bad) and placed back into trays or output media.

While, Strip form testing is a process wherein devices are tested while still attached to a panel or lead frame strip before they are singulated (cut into individual units). The entire strip is aligned and loaded into a handler for high-speed testing of multiple devices at once.

1.1 Advantages And Disadvantages Of Pick-And-Place Vs Strip Form Testing

PNP testing advantages are as follows: supports a wide range of package types and sizes, good contact quality with controlled insertion and ideal for low to medium volume and multiple product variations. While, disadvantages include slower throughput: mechanical pick and place actions limit speed, higher test cost per unit: due to slower speed and higher handling overhead and more manual handling and setup compared to strip testing.

Strip testing advantages are as follows: parallel testing allows faster processing of high volumes, lower cost per unit: efficient for high-volume manufacturing and well-suited for integration with automated back-end processes while disadvantages include requires standardized strip layout and compatible package types and limited to certain package types: Mainly for QFN and similar small form factor packages.

As semiconductor technology advances toward smaller, more compact packages like QFN, the traditional pick-and-place testing method is becoming less efficient for high-volume production. These miniature package types are well-suited for strip form testing, which offers greater parallelism, automation, and cost efficiency.

2. 0 REVIEW OF RELATED WORK

Refer to 1.0 Introduction.

3.0 METHODOLOGY

As semiconductor devices continue to shrink in size while increasing in complexity and production volume, traditional pick-and-place final test methods are becoming less efficient particularly for high-volume, small-package products such as QFN. In response to these evolving demands, the industry is shifting toward strip form testing, a method that enables parallel testing of multiple units while they remain in panel (strip) format prior to singulation.

Given this current situation, this paper is to tackle strategies to align with the evolving demands of the market and support next-generation products. This includes 1) design and full conversion to roadmap test solution, which uses below playbook as shown in Fig. 2.

Fig.2. Playbook for design and full conversion to roadmap test solution

(2) leverage strip solution from TI A/T sites, which uses below playbook as well as shown in Fig. 3.

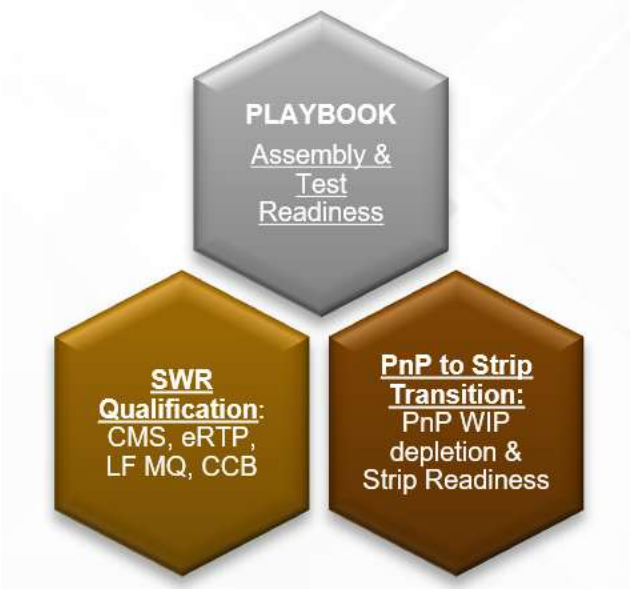

Fig.3. Playbook for leverage strip solution from TI A/T sites.

and (3) cost-efficient innovations: PnP to strip interposer solution and strip-to-strip hybrid contactor as shown in Fig. 4.

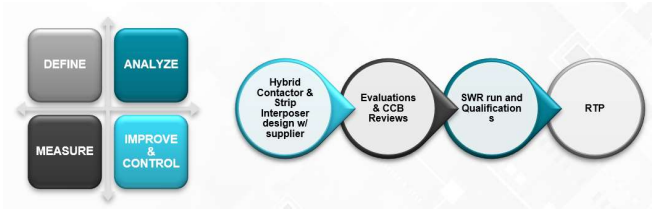

Fig.4. Playbook for cost-efficient innovations.

To support this transition, a structured and systematic approach is required to ensure successful conversion from pick-and-place to strip-based final testing. This methodology outlines the key strategies, technical considerations, and implementation steps needed to convert existing products and test infrastructure to a strip-compatible flow.

4.0 RESULTS AND DISCUSSION

Strategy 1. Design and full conversion to roadmap test solution

This roadmap outlines the phased strategy to transition from legacy Pick-and-Place (PnP) final test flows to a fully integrated, strip test-based solution, addressing both current production needs and future product scalability

Key elements of this strategy include: Capacity, Setup Requirement, OTC Saving Computations, BU Alignment, Test Hardware Design, Development, Test Plan, Program Conversion, SWR, Quals, PnP Depletion & Strip Readiness and RTP as shown in Fig. 5.

Fig.5. Key elements of Design and full conversion to roadmap test solution.

The Design and Full Conversion Roadmap is a strategic enabler for next-generation manufacturing, allowing the team to support modern packaging trends with a scalable, cost-effective test platform. Through cross-functional collaboration and structured execution, the team achieve a more agile and automated final test process that positions the team for long-term competitiveness in the semiconductor industry. Through this, 25 devices have been fully converted from PNP to Strip testing, as shown in Fig. 6, wherein activity has been maximized by increasing the number of sites and leveraging to roadmap testers as shown in Fig. 7.

Fig.6. PNP to Strip Conversion with multisite increase.

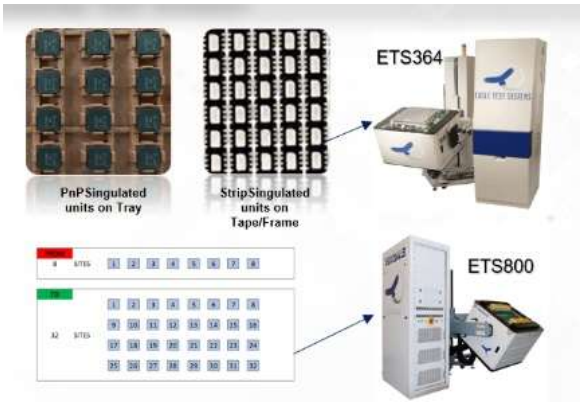

Fig.7. PNP to Strip Conversion with multisite increase.

The challenge on this strategy is the long cycle time for hardware design and development, engineering manpower & resources. So, a second strategy has been developed which is the leveraging strip solution from TI A/T sites

Strategy 2. Leverage Strip Solution from TI A/T sites

As part of the team's strategic shift toward high-efficiency, scalable testing, the team is exploring opportunities to accelerate strip conversion by leveraging proven strip test solutions from other manufacturing sites within the network. These solutions, already qualified and in production, offer a valuable foundation of technical know-how, validated hardware designs, and optimized test programs that can significantly reduce development time and risk.

By adapting existing strip platforms, the team aim to: standardize best practices across global sites, minimize redundant engineering effort, shorten time-to-production for new conversions, ensure consistent quality and performance across multiple regions.

This collaborative approach not only supports faster deployment of strip testing capabilities at th site, but also aligns with broader corporate goals for operational efficiency, knowledge sharing, and cost reduction.

Key elements of this strategy include: Identify PnP devices in Clark but Strip in other A/T site, Capacity, Setup Requirement Saving, OTC Computations, BU Alignment, Test HW Loan/ Purchase: LB, Contactor, Actuators, Recipes, Assembly Toolings, Lead Frame, Recipes, SWR, Qual, PnP Depletion and Strip Readiness, and RTP as shown in Fig. 8.

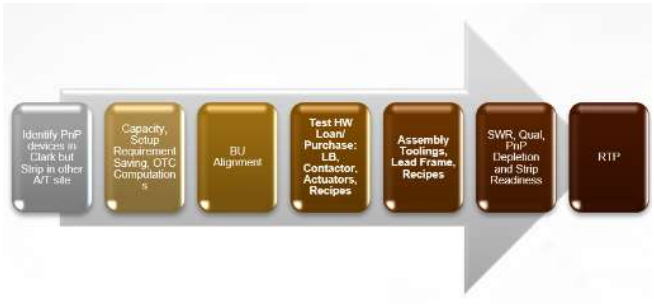

Fig.8. Key elements of leveraging strip solution from TI A/T sites.

Given this strategy, the team were able to identify high volume devices that are for strip qual at TI Clark as shown in Fig. 9.

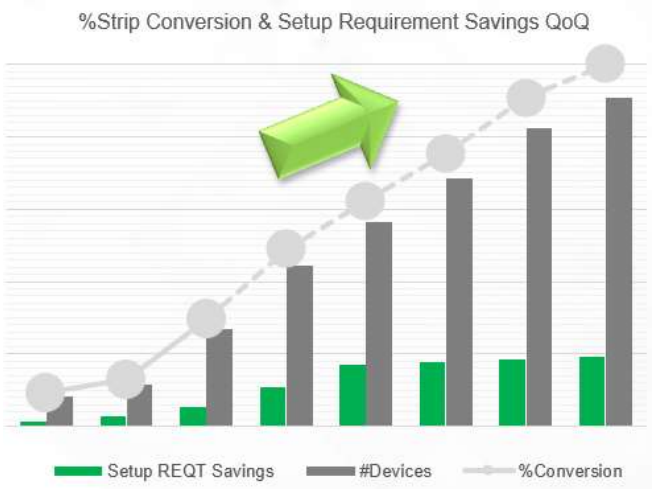

Fig.9. High volume devices identified that are for strip qual at TI Clark with existing strip solution from other A/T sites.

As the team move to leverage proven strip test solutions from other source site, it is essential to recognize and address key mechanical differences in package design that may impact strip compatibility and test performance. One critical variation lies in the lead frame saw street width: while the source site uses a 0.25 mm saw street, the local site (Clark) is currently utilizing a 0.35 mm saw street as shown in Fig. 10.

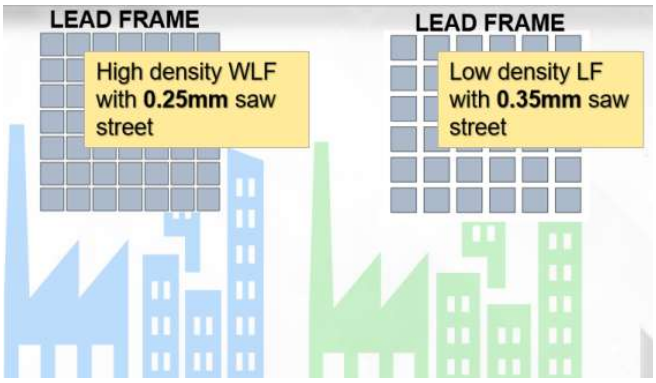

Fig.10. lead frame saw street width comparison from source area vs. TI Clark

This dimensional difference, though seemingly minor, has implications for: die pitch and strip layout alignment, contactor and socket positioning, test coverage and mechanical integrity and singulation and downstream automation compatibility

To ensure a successful transfer and adaptation of the strip solution, the team must evaluate and, where necessary, redesign aspects of the test hardware and strip configuration to accommodate the narrower saw street while maintaining electrical and mechanical reliability.

This introduction marks the start of the team's technical evaluation and engineering strategy to bridge these differences and fully integrate the strip test solution into Clark operations, and this is the third strategy.

Strategy 3: Cost-efficient innovations: PnP to strip interposer solution and strip-to-strip hybrid contactor

As part of the team's effort to align with the global standard and leverage existing strip test solutions, the team is transitioning from a 0.35 mm to a 0.25 mm saw street width in the lead frame design. This narrower saw street allows for tighter unit pitch, higher strip density, and improved test efficiency critical for supporting next-generation, high-volume semiconductor packages.

Rather than investing in entirely new test hardware such as custom load boards and contactors the team have taken a more cost-effective and agile approach by developing a hybrid contactor solution. This custom contactor is

engineered to accommodate existing 0.35 mm loadboard layout and the new 0.25 mm saw street leadframe configuration, enabling seamless compatibility with the existing load boards as shown in Fig. 11.

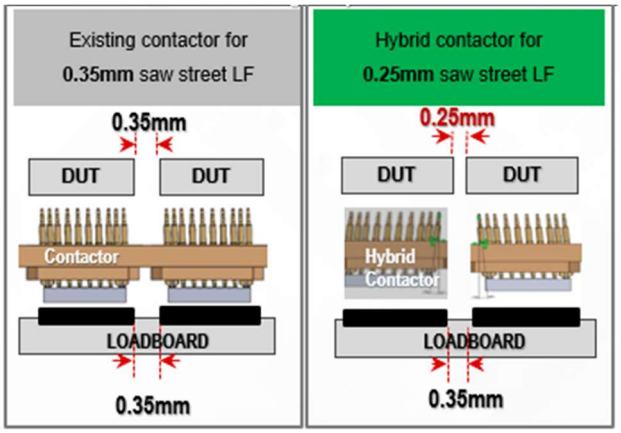

Fig.11. Hybrid contactor solution

The hybrid contactor approach offers several key advantages: reduced hardware cost and lead time, minimized disruption to existing test infrastructure, accelerated deployment of strip solutions using narrower saw streets, improved flexibility for multi-site or multi-package testing This introduction marks a critical step in enabling efficient, scalable, and cost-conscious adaptation of advanced strip test solutions within the local operations.

The potential risks considered included premature pin wear, shift in test readings, exposed copper, package cracks, and internal cracks. Each of these risks was carefully evaluated to determine their potential impact and likelihood. The assessment results were positive: module showed no signs of breakage, and also remained intact with no visible damage. In terms of electrical performance, resistance readings were stable and within expected limits, with all values indicating good continuity and no abnormalities detected.

In addition, as part of the team's strategic conversion from pick-and-place to strip form testing, the team is implementing a cost-effective solution to maximize reuse of existing PNP hardware. One key enabler in this transition is the development of an interposer that allows our current pick-and-place load boards to interface directly with the strip test contactor as shown in Fig. 12.

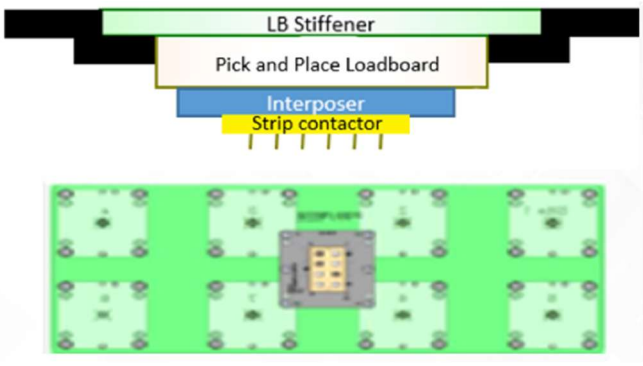

Fig.12. Cross section and top view of Interposer solution.

This interposer acts as a mechanical and electrical bridge, aligning the signal paths and physical interface between the pick-and-place designed load board and the new strip-format contactor. By using this modular approach, the team can: extend the life of existing load boards, avoiding immediate redesign and fabrication, accelerate time-to-deployment of strip test capability, reduce development costs while validating the strip solution, enable parallel support for both PnP and strip formats during transition phases.

The interposer strategy provides a flexible, scalable path for testing continuity while the team gradually ramp up full strip-dedicated solutions. It also offers a practical bridge during the learning curve of strip handler qualification and early production validation.

The implementation of the three core strategies marks a significant step forward in optimizing operational efficiency, align with the long-term business goals. The combined impact improves overall productivity for the local site as shown in Fig. 13.

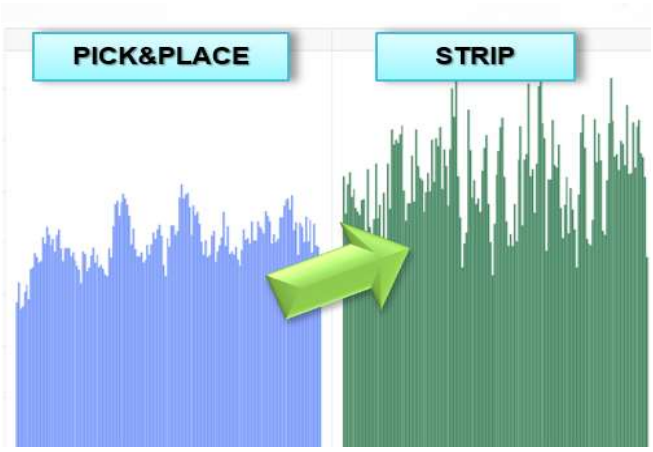

Fig.13. Daily output trend increased after strip conversion strategies and innovations

5.0 CONCLUSION

The strip conversion initiative delivered significant benefits across key performance areas. By enhancing Cost, Delivery, Innovation, and Quality (CDIQ), the project achieved substantial operational improvements and annual savings. Test coverage was notably expanded, while the transition led to broader strip volume adoption and reduced overall test cost requirements. Equipment displacement and reduced setup needs contributed to increased manufacturing efficiency and space optimization. Additionally, maintenance and setup efforts were dramatically reduced, further supported by successful lead frame harmonization. Overall, this transformation strengthened process capability and positioned the operation for sustained productivity and innovation.

6.0 RECOMMENDATIONS

To build on the success of the strip conversion, it is recommended to adopt the strip solution as the standard roadmap for future QFN offloads. Additionally, further studies should be conducted to evaluate the feasibility and reliability of high-temperature testing using Mylar thermal tapes. Exploring the potential for retest-on-strip capability is also advised to enhance test efficiency and reduce handling, contributing to continuous process improvement and cost savings.

7.0 ACKNOWLEDGMENT

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9.0 ABOUT THE AUTHORS

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