Solving Power Added Efficiency RF Degradation Issue on aHigh Frequency Doherty MIMIC Device Type in PQFN8X8 Package

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ABSTRACT

This report will discuss the different challenges encountered on the New Product Introduction (NPI) stage from the development phase to initial production run of BLM10D3740-35AB. This is a fully integrated high frequency asymmetrical Doherty MMIC device in PQFN8X8 package platform. The focus is to enhance the product's Radio Frequency (RF) performance specifically on the Power Added Efficiency at Middle Frequency (PAE_C_MF) solving the gross rejection issue at testing which will improve the overall yield. This is by Drain wire (Ld) loop height optimization through statistical approach and solving swayed wire issue by the implementation of rotated lead frame.

High frequency MMICs are susceptible to assembly-induced parasitic. This study aims to enhance the RF performance of BLM10D3740-35AB Doherty MMIC packaged in a PQFN 8X8 lead frame, through a Power-added efficiency at Middle Frequency (PAE_C_MIF). Failure analysis of the best-of-best (BOB) and worst-of-worst (WOW) samples revealed that excessive wire sway (>8%) and reduced wire pitch (<90um) among Ld3-Ld5, combiner wires contributed to performance loss, driven by loop height variation and mold-induced deflection. Results of the Design of Experiment (DOE) identified Ld4 loop height as a critical factor, with significant interactions from Ld3. Secondary assembly validation showed that rotating the lead frame 90 degrees relative to the mold flow minimized wire sway. This process changes improved PAE_C_MF stability, increasing the Cpk from 1.0 to 2.2 . These findings underscore the importance of precise wire control and wire-to-mold flow alignment in package assembly in achieving enhanced product RF performance.

1. 0 INTRODUCTION

Ampleon introduced the BLM10D3740-35AB MMIC solution with a 3-stage fully integrated asymmetrical Doherty configuration using state of the art LDMOS technology. The carrier and peaking device, input splitter, output combiner and pre-match are integrated in a single package. This multiband device is perfectly suited as a final stage for small cells and massive MIMO applications in the frequency range from 3700 MHz to 4000 MHz. This device is using a PQFN8X8 20 leads plastic molded package platform as shown on Figure1. This is die bonded using Silver sinter die attach process, and 27 wires bonded using 50ums diameter standard Al wire on a wedge bonding technology.

BLM10D3740-35AB Product Overview

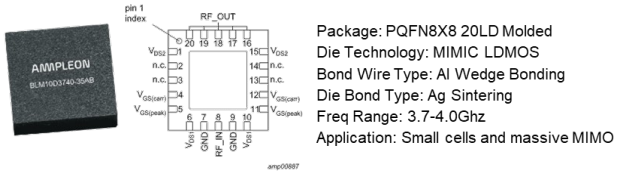

Figure1. Product Overview

Power-added efficiency on Middle Frequency at Carrier Amplifier (PAE_C_MF) is a RF test parameter that measures the efficiency of the amplifier at back-off taking into account the effect of the gain of the amplifier as shown on the formula below:

PAE_C_MF Formula:

$$PAE\_C\_MF = 100 \times \frac{(Pout\_C\_MF\_W - Pin\_C\_MF\_W)}{Vdnom * Ids\_C\_MF}$$

In the RF application, higher PAE means that the amplifier is converting more DC power into RF output, resulting in lower overall power consumption and improved efficiency. This translates into reduced cost, smaller packages and lesser heat to be dissipated, which is a very important aspect of mobile broadband devices.

Generally, at the product level in order to achieve the optimum performance in RF such as PAE, there are some key parts that need to be checked. These are the diffusion, die bond placement, and bond wires that are being controlled by die placement and wire calibration during assembly process as shown on Figure 2. These Ld wires with special loop profiles serve as a matching component to achieve the minimum power loss on the desired resonance frequency range.

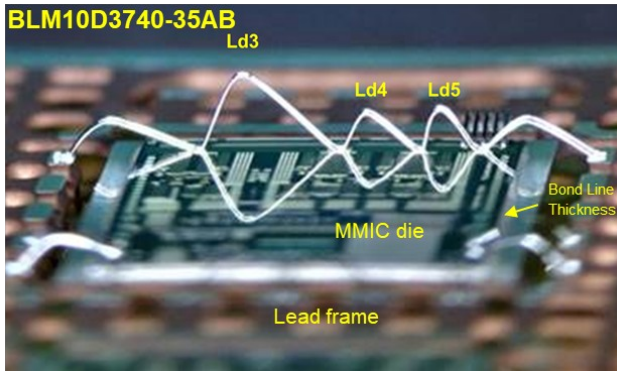

Figure 2 Product Configuration

Ld3, Ld4 and Ld5 wires in Figure 2 represent the combiner of the integrated Doherty. Their loop height accuracy and shapes are crucial for a high efficiency at back-off and can become more sensitive as we operate at high frequencies shown on Figure 3.

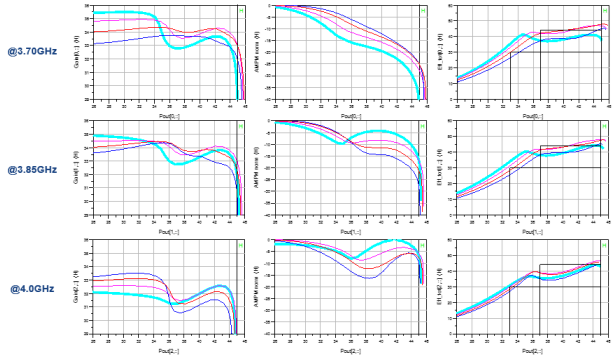

Figure 3 Simulation of Ld wires (+/-75ums) impact on RF performance on different frequencies.

The increasing demand for miniaturization and integration in RF systems really causes a lot of challenges in achieving good linearity and high power added efficiency (PAE) at higher frequency applications. For this device gross rejection of about 7.58% on PAE_C_MF was observed during the development phase which hampers the immediate release to Production.

2. 0 REVIEW OF RELATED WORK

Not Applicable.

3.0 METHODOLOGY

3.1 Statistical Screening

Statistical analysis was performed using Minitab to check the behavior of the PAE_C_MF spread. From the cumulative graph and histogram on Fig. 3 and Figure 4 respectively it can be seen that the spread is too wide with respect to the Test Limit where the values exceeded the lower specification limit (LSL).

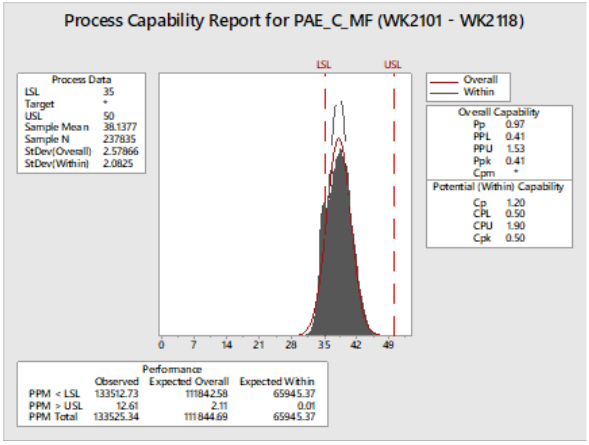

Figure 4 PAE_C_MF histogram.

3.2 Failure Analysis

Failure analysis was started by selecting the samples with PAE_C_MF Best of the Best (BOB) and Worst Of the Worst (WOW) values referring to the PAE_C_MF cumulative graph below.

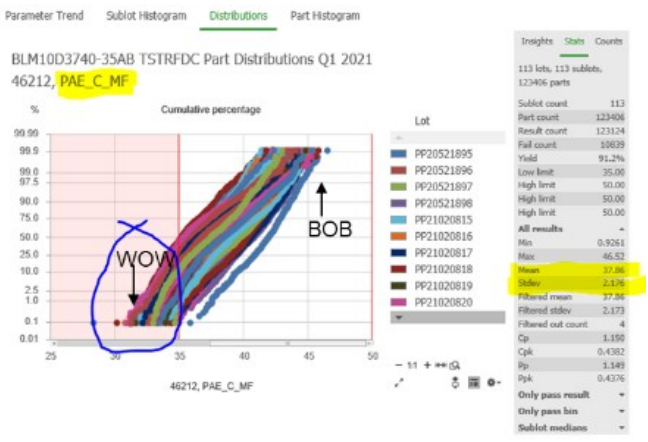

Figure 4 PAE_C_MF Cumulative Plot.

The first step was done by retesting the samples at RFDC, external visual inspection and then proceed for the mold removal by laser and chemical decapsulation to check the parts inside the device. After detailed visual inspection it was observed that most of Worst of the Worst (WOW) samples with very low PAE_C_MF at <32% showed swayed Ld3 wires > 8%. It can also be noticed that the gap in between the wires is very minimal, less than 90ums with respect to the adjacent Ld3 wire. For the Best of the Best (BOB) samples no physical irregularities were observed.

Wire sway is calculated by measuring the Wire Deflection then divided it by the Wire Span multiplied by 100 and the details. Wire Sway (%) = (Wire deflection / Wire Span)x100.
And wire pitch is the gap in between adjacent wires as can be seen in Figure 5.

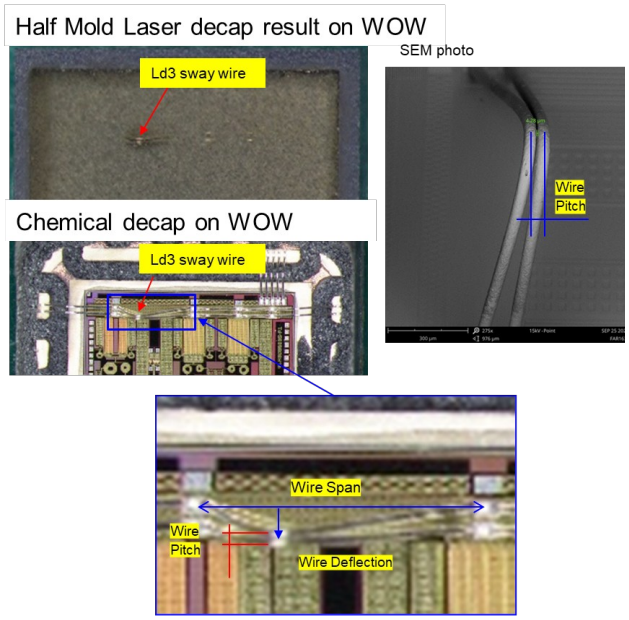

Figure 5 De-caped sample with very low PAE_C_MF

From the failure analysis result and cause and effect analysis performed, a validation plan was defined focusing on wire bonding and molding process. Two potential root causes were identified. 1st is the Ld loop height variation and the wire sway due to impact of mold flow on Ld wire resulting to a very close pitch/gap between adjacent wires.

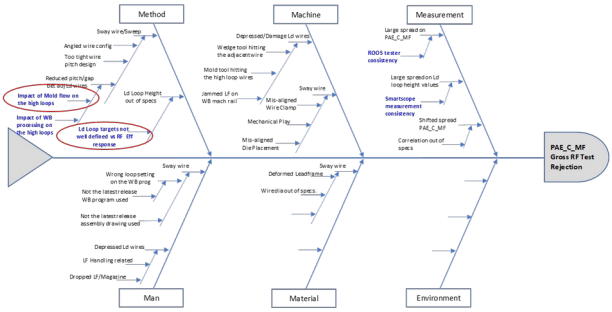

Figure 6 PAE_C_MF cause and effect analysis.

3.3 Wire Bond DoE

To assess the impact of Ld wire variation at Wire Bond (WB) and Wire Sway on PAE_C_MF, a Corner DoE was defined together with RF designer based on the initial RF simulation during development phase. On this experiment, different loop height variations were defined and also added intentional swaying of wire as shown on the Table 1.

Variant	Lot	LD3 height (um)	LD4 height (um)	LD5 height (um)	Marking (Line D)	Ld3 Wire Sway	Nb of samples
1	PE2115001200	1000	525	550	NOM	no	30
2	PE2115001201	1050	525	550	L3P	no	30
3	PE2115001202	950	525	550	L3N	no	30
4	PE2115001203	1000	575	550	L4P	no	30
5	PE2115001204	1000	475	550	L4N	no	30
6	PE2115001205	1000	525	600	L5P	no	30
7	PE2115001206	1000	525	500	L5N	no	30
8	PE2115001207	1050	575	600	ALLP	no	30
9	PE2115001208	950	475	500	ALLN	no	30
10	PE2115001209	1000	525	550	NOM_WS	yes	30
11	PE2115001210	1000	575	550	L4P_WS	yes	30
12	PE2115001211	1000	475	550	L4N_WS	yes	30
13	PE2115001212	1000	525	600	L5P_WS	yes	30
14	PE2115001213	1000	525	500	L5N_WS	yes	30

Table1 Wire bond Corner DoE runs with swayed wire.

Fourteen variants were built. Variant 1 to 9 are runs with +/-50ums loop heights on Ld3, Ld4 and Ld5 wires and for variant 10 – 14 variants are runs with loop height variation and intentionally swayed wires replicating the sway wire failure mode of PAE_C_MF seen on the failure analysis result. Ld3 wire pitch was also measured as an additional factor. Measurements are shown in Figure 6 and Figure 7 below.

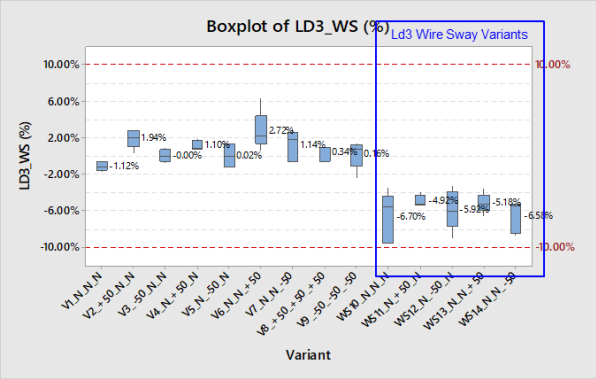

Figure 7 Box plot of Ld3 wire sway.

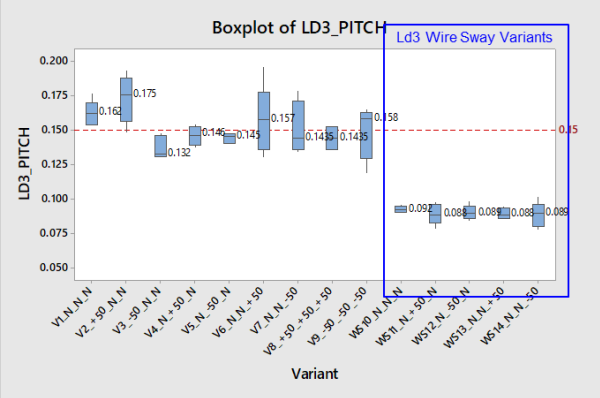

Figure 8 Box plot of Ld3 wire pitch.

3.4 Mold Flow DoE

The 2nd validation item is related to the impact of Mold flow with respect to the wire sway of Ld wires. Six variants were built, the Var1 and Var2 are control lots with normal orientation, Var3 and Var4 are rotated 90deg clockwise and Var 5 and Var6 are 90deg rotated counterclockwise with respect to the lead frame pinning configuration as shown on Table 2 and Figure 9.

Variant	Description	LF position on Mold tool	Qty	Assembly Drawing Version
Var1	Normal	Side A	30	BLM10D3740-35AB_Rev3_1
Var2	Normal	Side B	30	
Var3	Rotate 90° clockwise	Side A	30	BLM10D3740-35AB_Rev3_1 (Rot_Clockwise)
Var4	Rotate 90° clockwise	Side B	30	
Var5	Rotate 90° counter clockwise	Side A	30	BLM10D3740-35AB_Rev3_1 (Rot_Counter)
Var6	Rotate 90° counter clockwise	Side B	30	

Table 2 Leadframe Rotation vs Mold Flow Trial matrix

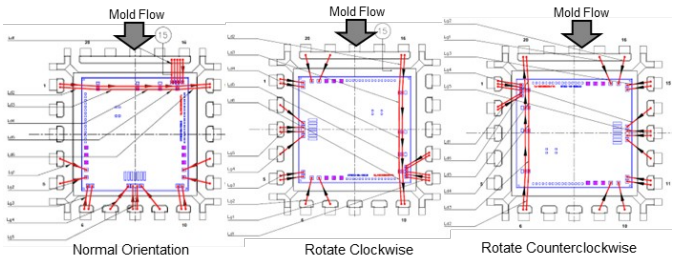

Figure 9 Wire and Die placement with respect to rotated leadframe configuration.

4.0 RESULTS AND DISCUSSION

Wire bond corner DoE was analyzed using General Factorial regression, Main effect plot and interaction plot. Based on the result the main factor that is influencing the PAE_C_MF is mainly on Ld4 variation which is directly proportional and inversely proportional on the Ld3 where P-values are below 0.05 as shown on Table 3, Figure 10 and Figure 11.

General Factorial Regression: PAE_C_MF+CorrDiff versus LD3, LD4, LD5, LD3 Pitch

Factor Information

Factor	Levels	Values		
LD3	3	0.948	0.993	1.048
LD4	3	0.475	0.522	0.57
LD5	3	0.505	0.55	0.595
LD3 Pitch	2	0.089	0.145	

Analysis of Variance

Source	DF	Adj SS	Total Adj SS	Adj SS (%)	Adj MS	F-Value	P-Value
Model	7	594.72			84.96	23.93	0
Linear	7	594.72			84.96	23.93	0
LD3	2	202.73	814.85	25%	101.363	28.55	0.000
LD4	2	484.63	814.85	60%	242.313	68.25	0.000
LD5	2	21.41	814.85	3%	10.703	3.01	0.056
LD3 Pitch	1	28.49	814.85	4%	28.486	8.02	0.006
Error	62	220.13			3.55		
Lack-of-Fit	6	82.2			13.699	5.56	0
Pure Error	56	137.93			2.463		
Total	69	814.85					

Table 3 General Factorial Regression Result for PAE_C_MF

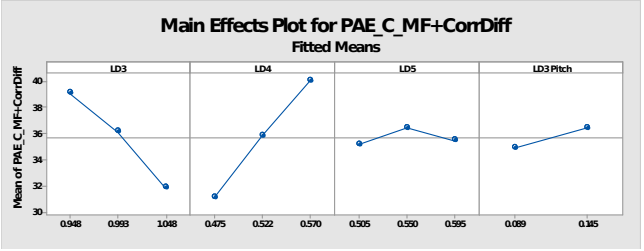

Figure 10 Main Effect Plots for PAE_C_MF

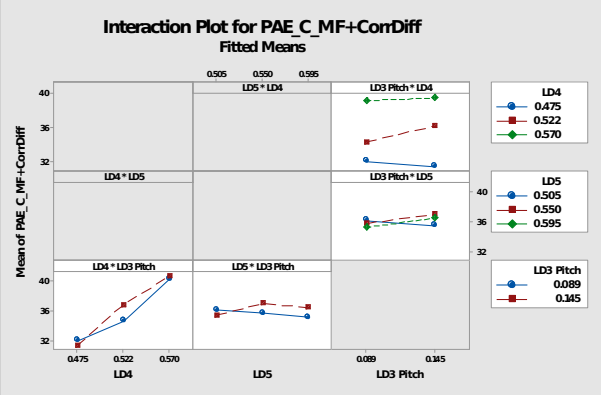

Figure 11 Interaction Plot for PAE_C_MF

For the impact of mold flow on different wire and die placement configuration, a comparative analysis using Anova on wire sway before and after Molding process was performed. Ld3 wire sway values with different wire rotation before molding, we don't see significant difference as the P-value is > 0.05. But after molding process a significant deflection of wires can be observed mainly from the Nominal samples shown on Figure 12 and Figure 13.

In general, for Normal wire placement, Ld3 and Ld4 exhibit significant difference in Mean and Std dev as expected. However, for rotated variants 90° clockwise and 90° counterclockwise NO significant difference can be observed. Wire bond placement in line with the mold flow either from 90° CW or 90° CCW with respect to the normal bond configuration have significantly lower wire sway and pitch values.

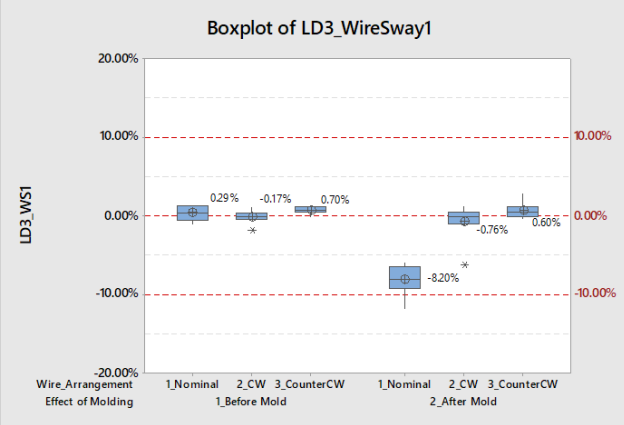

Figure 12 Boxplot of LD3 wire sway on different wire and die placement configuration.

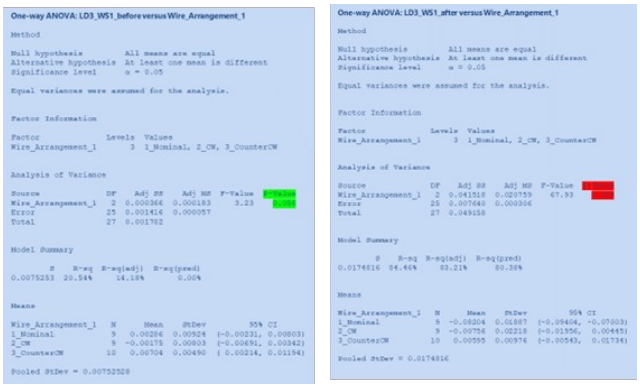

Figure 13 One-way Anova comparative analysis

After receiving the new rotated lead frame configuration, 20 actual lots were built using the normal leadframe and rotated leadframe from Assembly to Testing. Based on the statistical result the new leadframe. Based on the result, using the new leadframe the mean, standard deviation and CPK of PAE_C_MF significantly improved from 1 to 2.2 as can be seen on the Figure 14, Table 4 and Table 5.

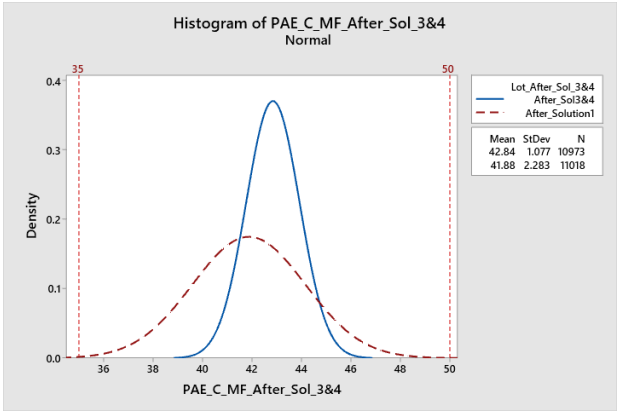

Figure 14 Histogram of PAE_C_MF on the normal and rotated leadframe.

Lot	Total count	Cpk	Yield (%)	Test yield (%)	Fail count	Mean	Stdev	Min	Max
PP21220713	1097	1.27	98.0	100	0	42.45	1.96	36.17	48.28
PP21220714	1099	1.20	98.3	100	0	42.54	2.07	36.26	47.30
PP21220715	1106	1.11	97.8	100	0	42.30	2.18	35.16	48.10
PP21220716	1108	0.80	98.3	100	0	40.63	2.35	35.14	46.61
PP21220717	1100	1.05	99.1	100	0	41.24	1.98	35.23	45.98
PP21220724	1096	1.20	100.0	100	0	41.88	1.91	35.46	47.36
PP21220725	1100	1.21	99.2	100	0	43.05	1.91	36.67	47.79
PP21220726	1105	0.85	99.3	100	0	41.15	2.41	35.24	47.20
PP21220727	1109	1.13	98.3	100	0	42.81	2.11	36.35	48.00
PP21220728	1096	0.84	97.9	100	0	40.69	2.25	35.24	47.04

Table 4 Lots using normal Lead frame.

Lot	Total count	Cpk	Yield (%)	Test yield (%)	Fail count	Mean	Stdev	Min	Max
PP22450413	1079	1.87	99.7	100	0	42.72	1.30	37.76	46.09
PP22481290	1093	2.84	99.9	100	0	42.41	0.87	39.44	44.61
PP22481627	1098	1.91	99.6	100	0	42.14	1.25	38.65	45.43
PP22481628	1088	2.25	99.9	100	0	42.90	1.05	39.05	45.98
PP22481629	1096	2.29	99.9	100	0	43.25	0.98	39.47	45.96
PP22481630	1089	2.67	99.6	100	0	42.79	0.90	39.61	45.36
PP22481631	1100	2.45	99.9	100	0	43.08	0.94	39.02	45.82
PP22481759	1095	2.90	99.8	100	0	42.77	0.83	39.97	45.05
PP22481760	1098	3.00	100.0	100	0	43.54	0.72	41.05	45.42
PP22481822	1106	2.24	98.6	100	0	42.89	1.06	39.52	45.76

Table 5 Lots using the Rotated Lead frame.

5.0 CONCLUSION

The observed PAE_C_MF degradation in BLM10D3740-35AB was attributed to Ld3 and Ld4 loop height variation and reduced wire pitch due to mold flow-induced wire sway. Statistical optimization using Minitab of wire loop height and leadframe rotation effectively mitigated these issues, improving the Cpk from 1.0 to 2.2 and reducing PAE rejections by over 80%. These findings are applicable to other high-frequency MMIC designs within the PQFN8X8 platform.

6.0 RECOMMENDATIONS

Since the design of this device is completely the same as the derivative type BLM9D3438-35AB, the improvement action can be fanned-out directly to make the PAE_C_MF RF test parameter more stable and robust.

Assembly Design Rule document for PQFN8X8 MIMIC types related to high loop height perpendicular to the mold flow needs to be reviewed and updated accordingly.

Wire Bond DoE model gives us the precise reference to further fine tune LD3 and LD4 loop height target to improve the PAE_C_MF but not deviating the released assembly drawing tolerance. This can be used as reference for future PQFN 8X8 MMIC designs.

7.0 ACKNOWLEDGMENT

The authors would like to thank the following who have contributed to the resolution of the problem:

- Emmanuel Urriza – NPI Product Engineer
- Ronald Lorilla – WB Process SME, Sr. Manager
- Jantzen Bobares – Midline SME, Director
- Percival Romulo – Test Sr. Manager
- Romeo Ventura – TDP, Sr. Engineer
- Aileen Perea – Process Control, Sr. Manager
- Malou Bigcas - Process Owner, Director
- Heman Paguio – Coach, Master Black

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2. C. Cosme, PQFN8X8 Assembly Design Rule Document.
3. BLM9D3740-35AB Ampleon Product datasheet

9.0 ABOUT THE AUTHORS

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Ferdinand M. Rabe, graduate of BS in Electronics and Communication Engineering from Technological Institute of the Philippines, Manila with 20 years' experience in semiconductor industry. Currently working as NPI STR/Project Management Manager, responsible for Sample Test

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