PACKAGE MINIATURIZATION THROUGH SUBSTRATE DESIGN AND ASSEMBLY PROCESS OPTIMIZATION – A PRODUCT COST REDUCTION CASE STUDY

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ABSTRACT

The demand for cheaper and smaller form factor semiconductor packages continues to grow with the increasing need for smaller, more powerful, and more efficient electronic devices. This paper presents a case study on leveraging various packaging optimization techniques to effectively miniaturize a wirebonded ball grid array (BGA) package while reducing cost.

Removal of depopulated balls, reduction of ball pitch, removal of passives, and implementation of new substrate technologies were the key techniques to miniaturization of the package which effectively reduced the package cost. Additionally, technology transfer to a high capacity facility further increased the cost saving – but not without risks that need to be addressed at the assembly facility.

The high capacity facility raised concerns at wirebond due to the smaller bond pad opening (BPO) compared to its current capability. To ensure quality requirements are met and high volume manufacturability (HVM) metrics are attained, capillary redesign and a design of experiment (DOE) to define the appropriate wirebond process parameters were performed to close the capability gap on bond pad opening.

The package size was effectively reduced from its original package size of 23mm x 23mm to 15mm x 15mm amounting to a 57% area reduction, and cost is 64% less than the original package size. All while retaining the pin count and functionalities.

1. 0 INTRODUCTION

Modern automotive and industrial systems favor smaller form factor and lower cost chips without sacrificing system performance. While there have been efforts to miniaturize the package at various stages of design, one needs to carefully select the flow based on the turnaround time, return on investment and overall effort [1]. This forces one to look at various options, in an industry focused way to reduce the cost at each stage of design development.

Challenges and solutions in redesigning a long running video processing product which was in a large wirebond BGA package with embedded passive components is discussed in this paper. The primary intent was to meet the demands of customers while decreasing production costs. Decreasing the package size posed challenges which include the selection of which miniaturization options to implement without sacrificing device functionality & quality, reuse of an existing die with a small bond pad opening.

Design requirements dictate the appropriate package type to choose. The previous design used plastic ball grid array (PBGA) package technology, which was the primary package choice for high input-output (IO) applications at the time. Fig. 1 shows the cross section of 4-layer BGA package using solder balls as interconnect between package substrate and board. This was a popular package technology for higher pin count devices and good thermal performance. However, this package technology requires thicker copper substrate layers leading to a thicker package making it more expensive due to material needs and processing challenges. The width and spacing of the traces are highly sensitive to the copper weight on the specific layer. Hence, achieving tighter pitch becomes difficult with increased thickness of Cu layer. Substrate vendors are also exiting this market and looking for different package options to shift towards low form factor which clearly PBGA cannot support. End equipment and modern electronics systems are also favoring smaller form factors, so overall PCB can be miniaturized leading to sleeker & more elegant system, lower system cost, and better design flexibility.

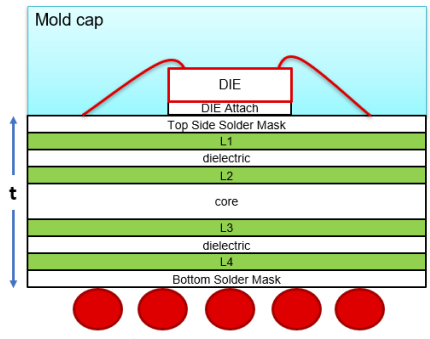


Fig. 1. Stack-up of a 4-layer substrate on a BGA Package

Hence, the parallel pursuit of cost reduction and miniaturization in recent years has increased emphasis on very small integrated circuit (IC) package solutions. The company produces a laminate-based family of CSP's known as New Fine Pitch Ball Grid Array (nFBGA) packages, an ideal solution to the cost reduction and miniaturization requirements. Because of their small body size, the bond wires are often shorter reducing the inductance. Their lower substrate thickness is attributed to using a thinner substrate material (see Table 1). They offer significant cost reductions compared to PBGA while boosting performance and without adding to system-level cost.

Table 1. PBGA vs nFBGA height and substrate thickness

Parameter	PBGA	nFBGA
Max height (um)	2352	1500
Substrate thickness (um)	560	308

In this case study, the authors targeted a cost-effective miniaturization by using the nFBGA package technology without losing functionalities. However, shifting from PBGA to nFBGA introduces certain challenges. For HVM, nFBGA size is currently limited to 17x17mm. To allow this, passive elements such as embedded decaps have to be removed. Also, reducing the overall body size causes signals to come closer and introduce crosstalk. The reuse of an existing die also introduces risk during potential HVM requiring optimization of current assembly tooling and processes.

2.0 REVIEW OF RELATED WORK

Not applicable.

3.0 METHODOLOGY

For any product, the total cost is contributed by three main aspects: die, packaging, and test – any of these options could be pursued for cost reduction. If a long running product has to be redesigned to decrease cost it also needs to account for redesign cost of die, which is a costlier and resource intensive undertaking with minimal return on investment. Meanwhile the test cost gets naturally optimized through years of high-volume manufacturing (HVM) experience. This leaves the optimization of package, via a lower cost derivative, as the only practical option.

3.1 Package size reduction options

Packaging is the one of the critical steps that could cost around 30% of chip cost. There are various factors affecting the package cost. On a high level it depends on material used (plastic/ceramic), pin configuration (leaded/area array) or assembly technique used (wirebond/ flipchip). The biggest factor that determines the package cost is the package size or the form factor. In this section we will go through various options available to arrive at a smaller size package.

3.1.1 Remove depopulated balls

Sometimes, balls are depopulated to accommodate passive elements (decaps) or to allow for board routing. If the design doesn't need passive elements and customers are okay with tighter board routing, it is recommended to fully populate the footprint by eliminating depopluated balls. Fig. 2. shows the 23x23mm pkg at 1mm pitch (left) vs 19x19mm pkg at 1mm pitch (right), each supporting 324 signals. This will preserve overall pin count while reducing pkg area by 31%.

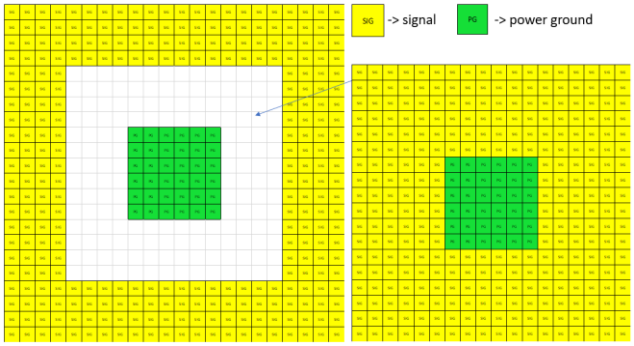


Fig. 2. Depopulated 23x23mm vs Full array 19x19mm ballmap

3.1.2 Reduce ball pitch

The ball pitch of a BGA package depends on the market requirement. Automotive customers prefer pitch above 0.65mm whereas for industrial markets 0.5mm is acceptable and consumer products accepts less than 0.5mm as well. By changing the pitch, the pin count can be increased within the same size or size can be reduced with the same pin count (Fig. 3). Finer pitch packages can still enable low-cost board routing rules by strategically depopulating balls to accommodate board escape routing and vias.

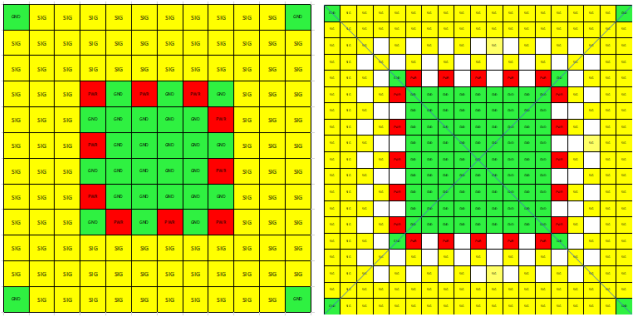


Fig. 3. 10x10mm 0.8mm pitch with 144 pins (left) and 10x10mm 0.5mm pitch with 293 pins (right)

3.1.3 Remove passive elements

In larger packages, the power delivery network (PDN) has to run for longer distances, hence accumulating more inductance thereby facing PI challenges. Often times to mitigate PI challenge, passive elements such as embedded decaps (Fig. 4) are introduced to provide stable power for critical domains. However, this will limit the package size based on the number of passive elements and their size. For better manufacturability these components have to follow stringent DRC rules. In case of decaps they should be placed a certain distance away from die edge and package edge which will limit the package miniaturization. Any package with embedded components will need to manage this routability overhead.

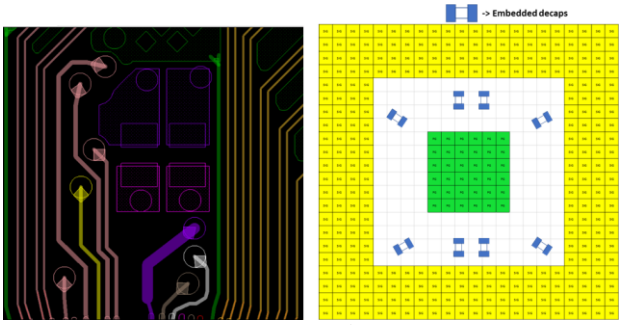


Fig. 4. Embedded decap on package (left) decap placement illustration (right)

3.1.4 Substrate manufacturing technology

In addition to the package size, the substrate manufacturing methods will also affect the cost. The number of substrate layers plays a critical role in substrate cost. If the design consists of high-speed signals and higher pin count, then additional power and ground planes are needed to overcome signal integrity (SI) and power integrity (PI) concerns.

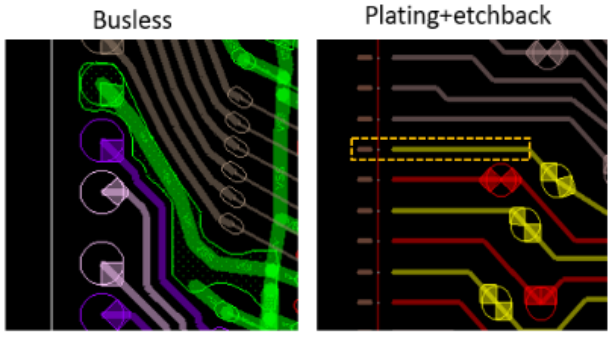


Fig. 5. Busless process (left) vs plating + etch back process (right)

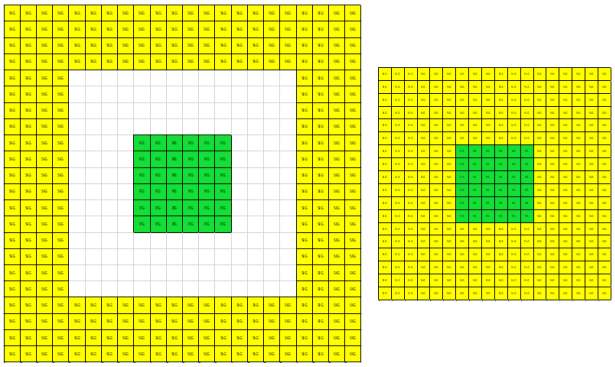
Similarly, the manufacturing process also varies with market that is being targeted. There are two prominent methods through which the substrate routings are manufactured: plating process and busless process. (Fig. 5) The former is the cheapest process but require more routing space, since every net has to be brought to the periphery of package through a plating bar. These edges cause copper corrosion and migration risk. To address it the team used an etch-back for the automotive market. Electrically the plating bars act as unterminated stubs and cause undesirable reflections degrading the timing margins. So, they should be codesigned within the tolerance. Whereas busless process is costlier and more suitable for extremely form factor constrained packages. Table 2. shows the cost difference for each option.

Table 2. Cost differences in processes

Parameter	Cost Increase
2L to 4L	~20%
Plating bar to Busless	~15%

3.2 Package miniaturization approach

The primary goal was to arrive at lower cost low form factor device. The original package is 23x23mm 1mm pitch, having embedded decaps and depopulated balls at center (Fig. 6). During the initial attempt, the entire foot print is populated, by removing depopulated balls and making it a full array. With this method, the size is limited to 19x19mm 1mm pitch package. However, for HVM, size of 17x17mm or lower is needed to shift for nFBGA technology. The main overhead is the presence of embedded decaps. Hence, the option of removing the embedded decaps which would enable a path towards 15x15mm 0.8mm pitch package which is within nFBGA manufacturability constraints was pursued.



(a) (b)

Fig. 6. (a) 23x23mm 1mm pitch (b) 15x15mm 0.8mm pitch ballmap

3.3 Wirebond assembly challenges

The package was previously assembled at a different facility with its own set of direct materials. As part of cost reduction, the new package is moved to a low cost HVM site with the lowest cost direct materials.

Reusing the die also pushed wirebond capabilities in terms of bond pad opening (BPO) at the HVM facility. The BPO is significantly lower than the qualified capability. To add more complexity, intrinsic to this die is a thick aluminum (Al) bond pad. Due to its soft characteristic, Al is easily displaced during wirebond leading to Al splashing (ALSP) (see Fig. 7).

This may cause shorts to adjacent metals such as bond pads, ball bonds, and ground rings. HVM assembly requirements ensure quality through a 100% ball on pad concept (see Fig. 8), wherein the ball bond formed together with its ALSP should be contained within the bond pad.

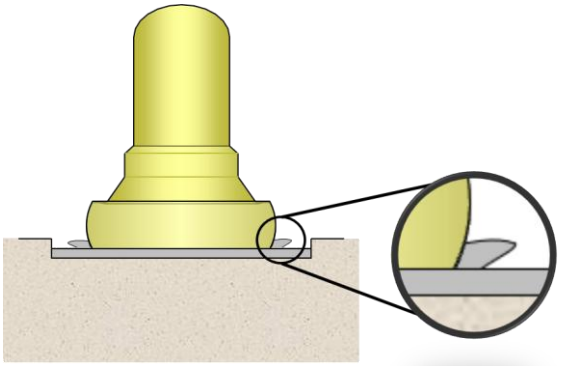


Fig. 7. Aluminum Splashing Visualization

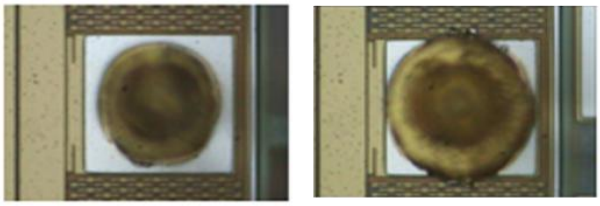


Fig. 8. 100% Ball on Pad - good vs reject

3.3.1 Challenges with ball bond

The ball bond diameter (BBD) is influenced by the combination of wire material & diameter, capillary dimensions, and the wirebond process parameters. All these factors significantly affect the resultant BBD and therefore meeting the BOP requirement.

In the previous facility, gold wire is used. To maximize cost reduction, copper wire is the proposed wire material which is significantly cheaper than gold. However, the change from gold to copper affects the wirebond process due to copper's greater hardness. This makes copper wire more prone to ALSP. To reduce the impact on ALSP, and also match gold's electrical conductivity, the copper wire diameter is reduced by 12% compared its gold wire version.

Even with the smaller wire diameter, there is a high and definite risk in non-compliance to 100% ball on pad requirement due to the combination of thick Al pad, hard copper wire resulting, and small bond pad opening. To ensure BOP compliance, a smaller ball bond diameter (BBD) needs to be defined.

To compute for the new target BBD, Al splash data were and collected from similar Si technologies with thick Al pads using copper wire. The maximum Al splash measured was incorporated into a series of BOP. The BBD which passed the 100% BOP simulation was considered as the new target BBD – calculated to be 30% lower than the old BBD target.

3.3.2 Wirebond capillary consideration

The assembly site has a set of capillaries already designed to be used based on the wire type and diameter which are selected based on bond pad opening, bond pad pitch, and electrical requirements. The capillary dimensions significantly impact the resultant BBD. The current capillary's chamfer diameter (CD) will result to a ball that is too large and cannot not satisfy the newly computed target BBD. The CD has to be designed to target the new BBD and ensure the best bond strength. Usually the BBD is ~1.2 greater than CD due to its geometry. Along with CD, another key capillary feature to re-design is the tip diameter (T). Since the bond pad pitch (BPP) is also smaller than current HVM capability, this requires the tip to be re-designed as well. This is to ensure that the capillary will not collide with the adjacent previously bonded wire.

Legend	
FA°	Face Angle
CA°	Chamfer Angle
H	Hole Diameter
T	Tip Diameter
CD	Chamfer Diameter
BNA°	Bottle Neck Angle
MTA°	Main Taper Angle
BNH	Bottle Neck Height
OR	Outer Radius
ITA°	Internal Taper Angle
TD	Tool Diameter
Mat'l	Tool Material
L'gth	Tool Length
ID	Internal Diameter
MD	Modified Diameter
VBH	Vertical BN Height

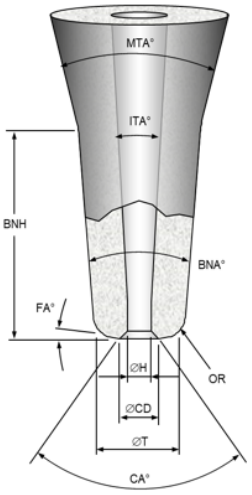


Fig. 9. Cross section of capillary

3.3.3 Capillary redesign

With the new target BBD and tighter BPP, multiple capillaries were designed (Fig. 10). *Cap Design 1* is the first iteration which incorporates a 10.7% smaller chamfer diameter (CD) and an 8.9% smaller tip diameter (TD) vs existing (old) design. However, its minimum achievable BBD does not meet the target BBD computed earlier – 8.3% larger BBD than required. The reduction in tip diameter already ensures no capillary collision to the previously bonded wire.

The second iteration, *Cap Design 2* retains the TD of *Cap Design 1* while further reducing the CD with a total of 18.9% reduction vs existing design. However, the equivalent

minimum achievable BBD is still slightly larger vs the target BBD.

The third and last iteration, Cap Design 3 retains the TD of Cap Design 1 and again further reduces the CD with a total of 21.4% reduction, respectively, vs existing design. The Bottle neck height (BNH) is also reduced by 16% reducing the USG transmission risk.

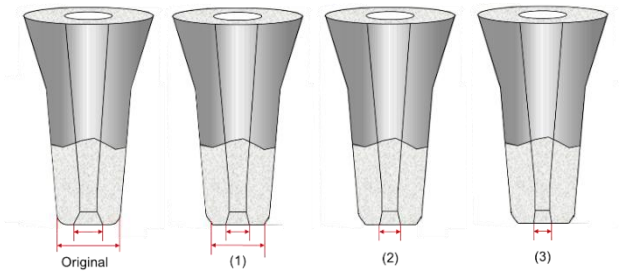


Fig. 10. Capillary designs considered

With these critical changes, the capillary dimensions were able to accommodate a smaller BBD, BPO and tighter BPP. In addition, to support this design further, a corresponding set of wirebond process parameters using the new capillary was then defined to meet the target BBD while minimizing Al splash. More details about parameter definition is described in next section. Aside from ball size and Al splash, additional risks include lifted ball bonds (LFBA) and low ball shear strength (BST).

3.3.4 Wirebond process parameters optimization

The wirebond process parameters consists of force, heat, and ultrasonic vibration (USG). The optimal combination of these wirebond process parameters is crucial for repeatable and high assembly yield for HVM. The Thermosonic bonding process requires force, heat, and ultrasonic vibration (USG) to successfully form a ball bond [7]. The combination of these factors influences the ball bond diameter, thickness, ball adhesion strength, and Al splashing. The industry standard way to optimize a set of wirebond process parameters that meets all of these requirements is through following method of design of experiments (DOE).

Effect Summary

Source	LogWorth	PValue
USG Current 1	6.953	0.00000
Force 1	1.497	0.03182
Force 3	1.357	0.04396
USG Current 3	1.314	0.04854
USG Current 2	0.952	0.11179
Force 2	0.919	0.12045

Remove Add Edit FDR

Fig. 11. Analytical results showing significant wirebond parameters

The significant factors were identified through a two-level screening DOE of various combinations of wirebond process parameters using an assembly analytical software tool (JMP). After various combinations of wirebond process parameters and collecting the output responses, USG Current 1, Force 1, Force 3, and USG Current 3 were the identified significant factors given their p-value (probability) of less than 0.05. See Fig. 11.

The resultant significant factors were then subjected to a full factorial DOE looking at all possible low and high value combinations of these factors. Their output response data were collected and was analyzed through JMP. A contour plot was created and a wirebond process parameter window was defined for USG1 and USG3 (Fig. 12). This defined parameter window ensures that all output requirements are met.

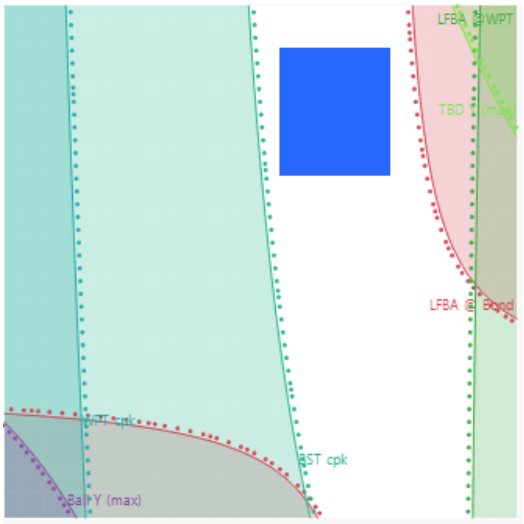


Fig. 12. Defined wirebond process window

4.0 RESULTS AND DISCUSSION

4.1 Package and Cost

Through implementation of various substrate technologies and taking advantage of new capability, the package size of the product was significantly reduced from 23mm x 23mm PBGA to a 15mm x 15mm nFBGA package – 57% size reduction without compromise to the device's pin count and functionality. The cost of the new package is also 64% lesser than its predecessor making up for significant cost reduction without significant investment in die redesign and test optimization.

4.2 Assembly validation results

After capillary design and wirebond process parameter definition was completed, bonded samples were subjected through several bondability test validations following internal standard manufacturability qualification requirements aligned with AEC-Q006 – group C package assembly integrity tests. Ball profile images show 100% ball on pad compliance with minimal splashing that is also still contained within the bond pad opening. Its bond shear strength also passed minimum strength requirements and passed in terms of its break mode.

Fig. 13. Bonded ball images after wirebond optimization

The bonded ball cross section also shows good bonded ball profile. Also demonstrated again is its minimal Al splashing. Bright field and Nomarski inspection were also performed to validate for any damage or cracking on the inter layer dielectric and the TaN layer – no signs of damage, cracks and compression. Through capillary redesign and wirebond process parameter definition, a robust and manufacturable process was defined. The key criteria of 100% ball on pad compliance was met. See figures Fig. 14 and Fig.15.

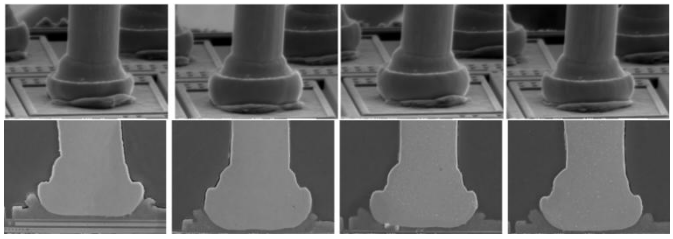


Fig. 14. SEM images of bonded ball (top) and cross section (bottom)

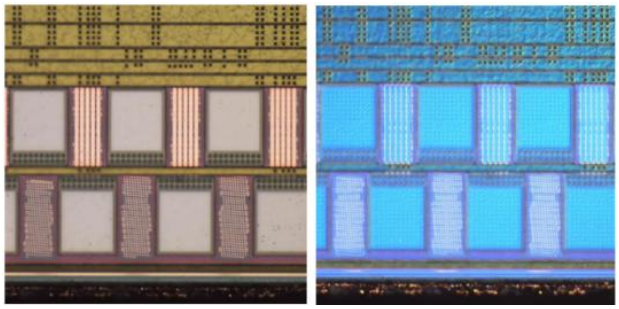


Fig. 15. Pad damage check: bright field & nomarski inspection

5.0 CONCLUSION

This work demonstrates a practical approach to improve the cost of a long running product through package miniaturization. Various substrate design approaches and technologies were combined together effectively and delivered a smaller size package without embedded decaps that still met the product performance requirement. The package size was reduced and effectively reduced the cost of the package.

The HVM assembly line challenge of accommodating tighter BPO and BPP was also resolved through a systematic approach to capillary and wirebond process optimization.

The capillary redesign approach and validation techniques gives a blueprint to meet assembly reliability spec when pushing for tighter bond pad openings. Package, Board and Assembly co-design ensured a first pass success while minimizing system cost of customers. The study enabled the company to meet the demands of customers to provide smaller form factor and cost-optimized products for their future systems. Smaller form factor package also opens up new opportunities in the evolving automotive and industrial market space which were not present when the earlier version of the product had sampled.

6.0 RECOMMENDATIONS

The power integrity and signal integrity changes due to the drastic change in the package size will be further studied by the authors. This future study will include the risks on power integrity and signal integrity as well as their corresponding mitigation techniques.

7.0 ACKNOWLEDGMENT

This study was supported by Texas Instruments. The authors would like to thank the ASM Auto Business Unit & Co-design Team, and the Texas Instruments (Philippines), Inc. – Asia Packaging & Test Execution (TIPI-APTE) Team for their contributions to this study.

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9.0 ABOUT THE AUTHORS

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10.0 APPENDIX

None.