OPTIMIZING SEMICONDUCTOR PERFORMANCE: PACKAGE RESISTANCE REDUCTION THROUGH BOM AND PARAMETER ENGINEERING

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ABSTRACT

Reducing package resistance in the "Single Channel High Side Driver Switch Devices" family is critical for both product and package development. High resistance negatively affects performance and efficiency, leading to increased power consumption, slower operation, and overall inefficiency in switching load applications. Therefore, minimizing resistance is essential to enhance device reliability and operational effectiveness, ensuring optimal performance under various conditions.

This study examines how assembly Bill of Materials (BOM) components and process parameters affect resistance in switching load application devices. Key factors analyzed include wafer/die thickness, Bond Line Thickness (BLT), wire diameter, and the number of wires. Drain-source on-resistance (RDSON) data from final tests were evaluated using statistical software to identify the most effective configurations. A Design of Experiment (DOE) was conducted on die bond and wire bond to verify the manufacturability of the identified configuration. Reliability tests, including UHAST, TC, and HTSL, were also performed to confirm that the selected configurations-maintained performance integrity under various stress conditions.

Experimental results showed that thinner dies, increased BLT, thicker wires, and additional wires significantly reduced overall package resistance. By leveraging these innovations, the team successfully met the customer's product requirements. This achievement is projected to generate substantial revenue by 2033, driven by the launch of approximately 20 products within this device family.

1. 0 INTRODUCTION

In the realm of semiconductor technology, reducing resistance is a pivotal challenge that significantly influences device performance and efficiency. High resistance in semiconductor devices can lead to increased power consumption, diminished operational speed, and overall inefficiency. These issues underscore the necessity for effective strategies to minimize resistance, thereby enhancing device reliability and operational effectiveness across various conditions.

Considering the die's maximum design capability for resistance targets and the package portfolio's design rule limitations, the challenge is to reduce overall resistance through BOM selection and process optimization to meet customer requirements. This paper explores the optimization of assembly BOM components and process parameters to achieve lower resistance in the "Single Channel High Side Driver Switch Devices" family. By analyzing factors such as wire thickness, die size, bond line thickness, and the number of wires, this study aims to identify configurations that significantly reduce resistance

1.1 Understanding RDS (on) in Semiconductor Devices

One key parameter in evaluating the resistance of semiconductor devices is the drain-source on resistance (RDSON). RDSON is the resistance between the drain and source terminals of a Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) when it is in the "on" state. [1] This resistance is crucial because it directly affects the power loss and efficiency of the device. Lower RDSON values are desirable as they lead to reduced conduction losses and improved overall performance. See Figure 1

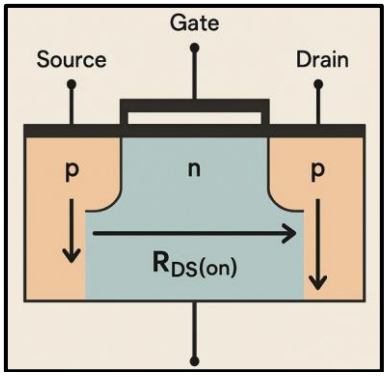

Fig. 1. Simple RDS (on) Diagram. The illustration of RDS (on) in MOSFET devices shows the resistance between the drain and source terminals.

2. 0 REVIEW OF RELATED WORK OR LITERATURE

The study began by adopting a theoretical approach to understanding the resistance characteristics of MOSFETs. This initial phase involved comprehensive research, simulations and analysis of the fundamental principles governing MOSFET resistance, particularly focusing on the theoretical aspects of RDSON.

Existing literature and mathematical models were reviewed to predict the behavior of RDSON under various conditions. This theoretical groundwork provided a solid foundation for the subsequent experimental phase. The mathematical model R=ρLA$R=A\rho L$ guided us in selecting materials with lower resistivity (ρ), as it is directly proportional to overall resistance. Additionally, increasing the cross-sectional area (A) helped reduce resistance [2].

$$R = \rho \frac{\mathrm{L}}{\mathrm{A}}$$

where:

- R is the resistance,
- ρ is the resistivity of the material,
- L is the length of the material,
- A is the cross-sectional area.

Numerous studies have been successfully published in reputable journals related to package resistance. Fang Qu found that substituting the EMC material with one that has higher thermal conductivity can enhance the heat dissipation performance of the package, particularly by lowering the thermal resistance of the outer layer. Additionally, increasing the thickness of the die can also contribute to better heat dissipation, although the improvement is relatively minor [3].

Hiroshi Kono study focused on enhancing the tradeoff between specific on-resistance and short circuit ruggedness of 1.2-kV-class SBD-embedded SiC MOSFETs by reducing cell pitch and optimizing internal resistance [4].

Another study examined Tae Yeong Hong the impact of using graphene as an interfacial layer between Cu electrodes and graphene channels to lower contact resistance and enhance adhesion energy, which are essential for high-performance interconnects and bonding in advanced semiconductor devices [5].

While many factors influence resistance, this study focused exclusively on the role of assembly in reducing overall package resistance in a switching load application device.

3.0 METHODOLOGY

Discussed in this section are the materials and equipment used throughout the study and a general description of the methods involved.

3.1. Materials & Equipment

The new device technology being developed uses Damascene Copper Top Metal die technology with a three-layer metal structure and a 4.0µm Front Metal Thickness (FMT) for smart switch applications. It is fabricated on an 8-inch wafer and packaged in a TSSOP exposed pad format.

The device faces challenges in resistance and thermal conductivity, making standard die attach epoxy insufficient. Therefore, sintered Ag and solder paste are being considered as alternatives. For wire bonding, Au PCC is selected to meet Grade 1 reliability requirements, with wire suppliers chosen based on wire resistivity. The mold compound used is the standard for automotive applications.

Before assembly evaluation, machines were carefully selected for optimal bonding of new materials. For die attach, the AD838 from ASM was chosen for its up-looking inspection systems, enhancing placement accuracy and die integrity. For wire bonding, Conn X from KNS, GoCu from ASM, and UTC5k from SKW were evaluated. The UTC5000 from SKW was chosen for its screwless transducer, precise bond force calibration, and controlled XY table vibration.

3.2. Die Thickness and Wire Size Selection

Based on product simulations and considering the maximum die size allowed by lead frame design limitations and design rules, we studied the impact of die thickness and wire size on overall package resistance. Samples were built using baseline assembly parameters to compare 30 RDSON readings after the final test, examining 4 mils and 6mils die thickness and 2.0 mils and 2.5 mils wire diameter. The study also included variations in Bond Line Thickness (low BLT vs. high BLT) and the number of wires (4 wires vs. 8 wires).

Table 1 shows the summary of experimental combinations.

Table 1. Summary of Experimental Combinations

Parameters	Condition 1	Condition 2
Die Thickness	4mils	6mils
Bond Line Thickness	Low	High
Wire Diameter	2.0mils	2.5mils
Number of wires	4 wires	8 wires

3.3. Manufacturability

Based on the final RDSON test results, the optimal configuration of the Bill of Materials and process parameters was identified. Using this combination as a baseline, a Design of Experiment (DOE) for die bonding and wire bonding was initiated, while chipping performance was validated using well-established parameters from other sites for the wafer saw process. A comprehensive DOE plan was developed to ensure overall quality effectiveness for critical responses such as Bond Line Thickness (BLT), epoxy coverage, tilt, fillet height, and voids in the die bonding process. Initial screening of parameters was conducted to identify factors causing bond pad cracks during wire bonding of thick copper wire, followed by an analysis of factors affecting ball size, Intermetallic Coverage (IMC), and Pad Metal Displacement ratio (PMDr). Refer to Appendix A and B for the detailed DOE plans for die bond and wire bond processes, respectively.

Most responses were analyzed using optical microscopy and scanning electron microscopy (SEM). A delayering process was conducted to inspect wire bond cracks due to the use of thick wire. These techniques also assessed potential damage to underlying structures after removing the bond pad metallization.

3.4. Reliability

After completing manufacturability testing through a series of DOE at time zero, a reliability test was conducted to evaluate the effectiveness of the configuration after stress.

- Unbiased Highly Accelerated Stress Test (UHAST) - 130°C, RH 85%, 18.8psi for 192hrs
- Temperature Cycle (TC) – (-) 65°C / 150°C for 2000 cycles
- High Temperature Storage Life (HTSL) – 175°C for 2016hrs

To evaluate the assembly's performance under diverse conditions, Custom Destructive Physical Analysis (CDPA) techniques were utilized. These analyses primarily employed Scanning Acoustic Tomography (SAT) to assess delamination following Thermal Cycling (TC). The presence of residual aluminum was examined post-Intermetallic Compound (IMC) growth and after High-Temperature Storage Life (HTSL) testing. Additionally, signs of corrosion were investigated following unbiased Highly Accelerated Stress Testing (uHAST).

4.0 RESULTS AND DISCUSSION

4.1. Die Thickness and Wire Size RDSON results

The selection process began with configuring die thickness. Based on the final test results, the RDSON for 4mil die thickness is significantly lower and, hence, better, compared to 6mil die thickness, with a p-value of 0.0001. Refer to Figure 2.

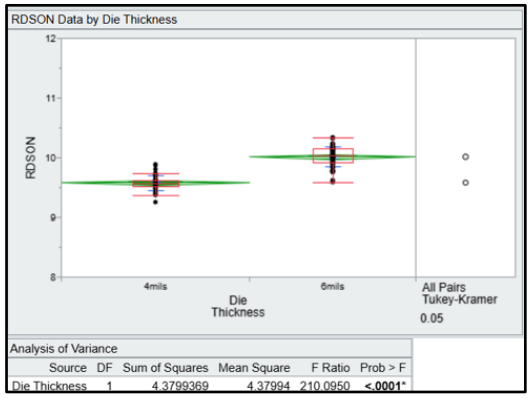

Fig. 2. RDSON Data Based on Die Thickness. The data shows that the RDSON of a thinner die is significantly lower than that of a thicker die.

Secondly, after establishing the die thickness, the wire size selection was addressed. The results indicated that a thicker wire (2.5 mil) is superior to a thinner wire (2.0 mil) for wire bond interconnect configuration. This finding is statistically supported with a p-value < 0.0001. Refer to Figure 3.

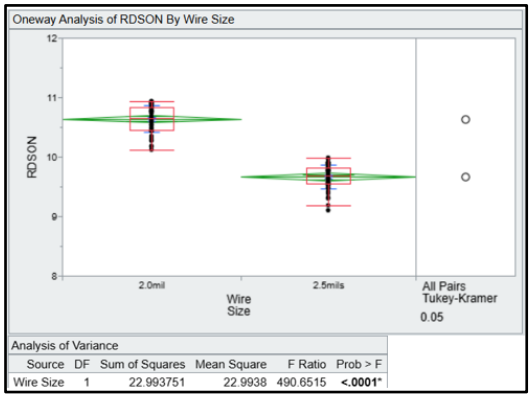

Fig. 3. RDSON Data Based on Wire Size. The data indicates that a thicker wire results in a lower resistance value compared to a thinner one.

Next, after identifying the optimal die thickness, the results for Bond Line Thickness (BLT) indicated that a low BLT is not advantageous for reducing resistance. Normal BLT results showed significantly lower resistance compared to low BLT, with a p-value of 0.0059, as shown in Appendix C.

Lastly, after determining the optimal wire diameter, it was observed that increasing the number of wires further reduces resistance. This was validated by comparing the RDSON results of configurations with 4 wires and 8 wires. The RDSON for 8 wires was significantly lower than that for 4 wires, with a p-value < 0.0001, as shown in Appendix D.

Experimental results from the RDSON comparison indicate that thinner die sizes, increased BLT, thicker wires, and an increased number of wires significantly reduce resistance.

After identifying the optimal die thickness and BLT target for the die bond process, Sintered Ag was chosen as the compatible material for the die bond paste to match the lead frame surface. The Technical Data Sheets (TDS) for both Sintered Ag and Solder Paste confirmed that they met the thermal conductivity requirements. For the wire bond process, after determining the wire size and the required number of wires, the wire supplier was selected based on the wire resistivity data from the TDS. An actual RDSON comparison was then conducted following this careful selection. The results, shown in Appendix E, confirmed that wires with low resistivity ensure better RDSON readings.

4.2 Manufacturability Results

The manufacturability of these configurations was optimized on the assembly line (wafer saw, die bond, and wire bond), as the thin die (4mils thickness) with backside metal and thick Au PCC wire (2.5mils) are new to onsemi, Carmona.

4.2.1 Wafer Saw

Benchmarking studies from various sites were consolidated to optimize the wafer saw process for 4 mil die thickness with backside metal. The analysis concluded that a step cut process yields the best results in terms of chipping performance, as illustrated in Figure 4. Additionally, implementing this optimized process has shown consistent product quality without sacrificing productivity.

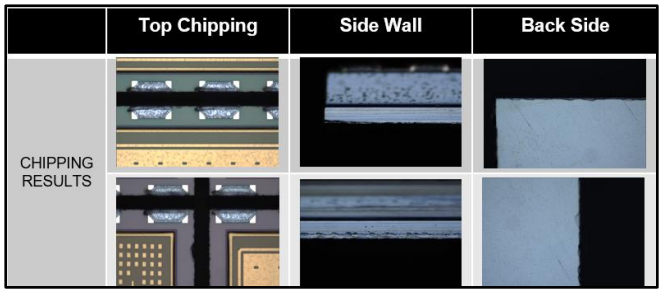

Fig. 4. Wafer Saw Chipping Results. The data shows that the top, side wall, and back side chipping passed all the target criteria.

4.2.2 Die Attach

During the comprehensive DOE, parameter screening results indicate that dispense pressure, bond force, and bond delay significantly impact the critical responses identified in the DOE planning phase. The prediction and contour profiler tools help define the optimal process window during the optimization phase. Refer to Figure 5.

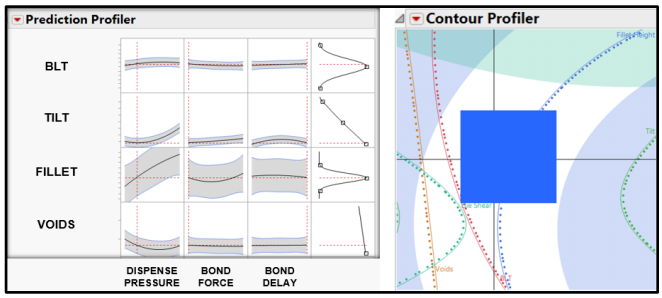

Fig. 5. Prediction and Contour Profiler. The profiler illustrates the impact of each input variable on the critical output response and indicates the parameter window that can be utilized during the validation phase.

Process window parameter validation was conducted based on the window defined during the optimization phase. The results were satisfactory across multiple metrics, including Epoxy Coverage, Fillet Height performance, Tilt, and voids, as shown in Figure 6.

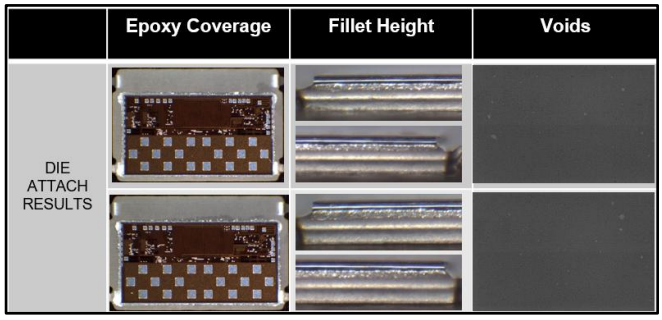

Fig. 6. Die Attach Output Response. The defined process shows consistent passing results in terms of die bond critical output response.

Bond Line Thickness, which is one of the critical output responses at die bonding passed and within target specification as discussed on Figure 7.

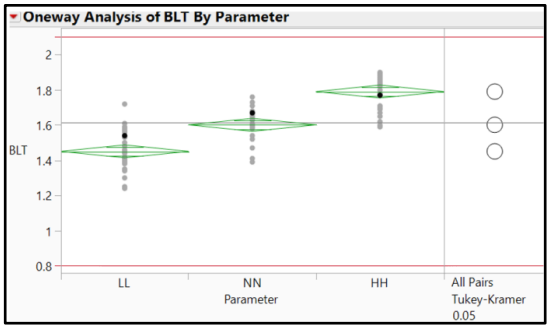

Fig. 7. Bond Line Thickness results. After defining the process window, the data of BLT consistently falls within the target range.

4.2.3 Wire Bond

During wire bond full DOE, results from the parameter screening phase indicated that S1 Force, S2 Force, and S2 US Power are significant factors to consider in the initial evaluation phase. It was also confirmed that any amount of scrub leads to bond pad cracks when working with thick PCC wire. See Figure 8.

	Parameter Setting					Result
	S2 US Power	S2 Bond Force	S1 Bond Force	Scrub Cycle	Scrub Width	Crack
Leg 1	Extreme Low Setting			Without		Passed
Leg 2	Extreme High Setting			Without		Passed
Leg 3	Extreme Low Setting			With		Failed
Leg 4	Extreme High Setting			With		Failed
Leg 5	High	Low	Low	With		Failed
Leg 6	High	High	Low	With		Failed
Leg 7	Low	Low	High	With		Failed

Fig. 8. Parameter Screening for Cracks. The evaluation results indicate that any amount of scrub applied can cause damage to the bond pad.

In the subsequent optimization phase of the DOE, the contour profiler defines the process window based on the factors identified during the screening phase as illustrated on Figure 9.

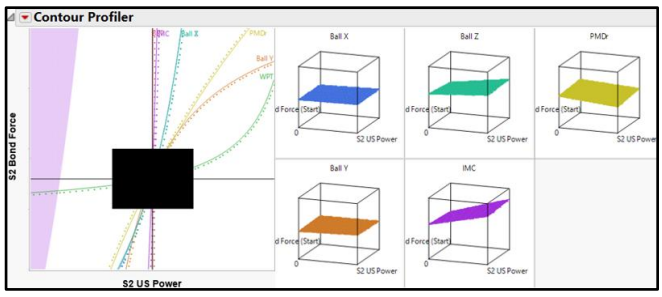

Fig. 9. Wire bond DOE Contour Profiler. The tool showed the recommended optimal parameter window (black box) that can be utilized during the validation phase.

The final validation phase demonstrates that the defined window from the identified factors yields passing results for ball size and formation, with sufficient aluminum remaining. Most importantly, the intermetallic coverage (IMC) passed with no cracks observed. Refer to Figure 10.

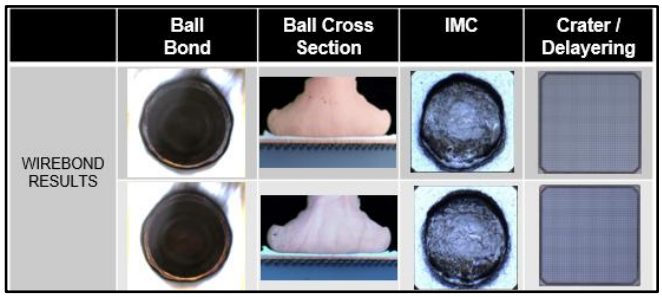

Fig. 10. Critical Wire Bond Output Data. The data of ball formation, supported by the cross-section, passed with no cracks observed after Time-0 data evaluation.

4.3 Reliability Results

4.3.1 Unbiased Highly Accelerated Stress Test (uHAST)

The Unbiased Highly Accelerated Stress Test (uHAST) yielded reliable results using the defined configuration set from assembly. No signs of delamination in any region were observed in the Scanning Acoustic Tomography (SAT) results after 192 hours. See Figure 11.

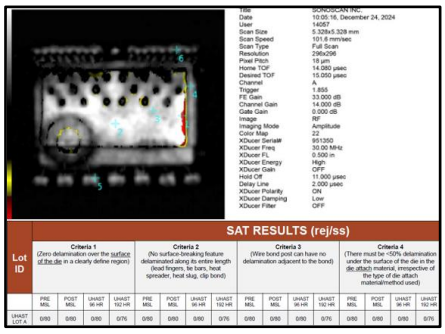

Fig. 11. SAT Data after U/HAST 192 hrs. The data revealed no abnormalities, and no sign of delamination was observed in all regions.

Additionally, no evidence of corrosion was detected in the cross-section results, particularly at the bond interface, after 192 hours of uHAST as shown in Figure 12.

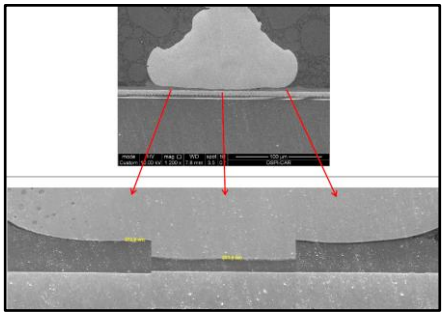

Fig. 12. SEM Cross-Section Photos after U/HAST 192hrs. The data revealed no abnormalities, and no sign of corrosion was observed.

4.3.2 Temperature Cycle (TC)

The Temperature Cycle (TC) testing also yielded positive results. No electrical failures were observed after 2000 cycles, confirming that no material separation occurred. The electrical test data also verified that there were no issues with die cracks due to the thin die. Additionally, there were no signs of delamination in any region, demonstrating the compatibility of the selected materials and the robustness of the defined process illustrated on Figure 13.

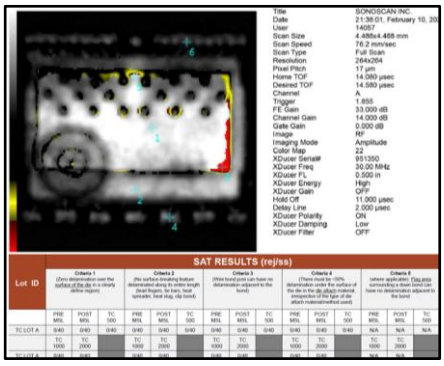

Fig. 13. SAT after TC 2000 Cycles. The data revealed no abnormalities, and no sign of delamination was observed.

Any potential cracks were also inspected after 2000cycles at TC, and no abnormalities were found, see Figure 14.

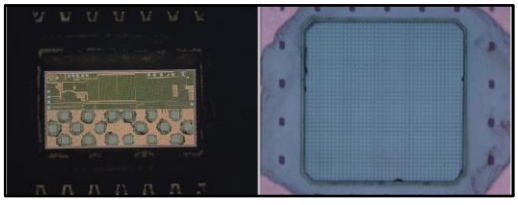

Fig. 14. Magnified Image of Ball Bond after TC2000 Cycles. No underlying pad damage was observed.

4.3.3 High-Temperature Storage Life (HTSL)

The High-Temperature Storage Life (HTSL) tests revealed no failures, starting from the electrical tests post-stress and including all CDPA results. Acceptable aluminum residues were observed after 2016 hours, indicating a controlled wire bond process with a wire thickness of 2.5 mils illustrated on Figure 15.

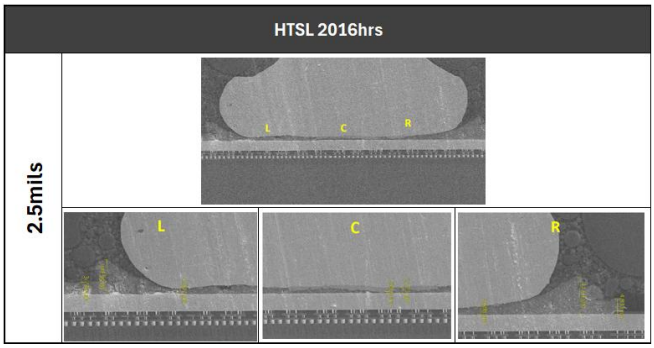

Fig. 15. 2.5mils Ball Bond Cross-section Photos after HTSL 2016hrs. The images reveal good ball formation with aluminum residues remaining after IMC growth.

Experimental results showed that thinner dies, increased BLT, thicker wires, and additional wires significantly reduced overall package resistance. By leveraging these innovations, the team successfully met the customer's product requirements. This achievement is projected to generate substantial revenue by 2033, driven by the launch of approximately 20 products within this device family.

5.0 CONCLUSION

The study successfully identified key assembly Bill of Materials (BOM) components and process parameters that significantly reduced resistance in load switching application devices, as detailed in section 4.1. By optimizing wafer/die thickness, Bond Line Thickness (BLT), wire diameter, and the number of wires, the research demonstrated significant improvements in RDSON values. Furthermore, the manufacturability of these configurations was validated through comprehensive design of experiments, ensuring practical application in semiconductor assembly processes. Reliability testing, including UHAST, TC, and HTSL, confirmed the performance integrity of these optimized configurations under various stress conditions.

6.0 RECOMMENDATIONS

To further reduce the package resistance of "Single Channel High Side Driver Switch Devices," it is recommended to consider several assembly factors in addition to die thickness, wire size, Bond Line Thickness (BLT), and the number of

wires. Selecting materials with lower resistivity for the lead frame and optimizing its design can significantly reduce resistance. Implementing advanced lead frame designs that enhance electrical conductivity will contribute to improved device performance. In addition, evaluating the impact of different package types on resistance and selecting the most appropriate one for specific applications can enhance device performance.

The authors also recommend investigating the potential nonlinear effects of the die bond and wire bond factors on their respective output response. Currently, the response modeling is limited to linear terms due to resource constraints

7.0 ACKNOWLEDGEMENT

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10.0 APPENDIX

A. DOE Plan for Die Bond Process

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Design of Experiment PLAN

Experimental Objective/s	
	Comparison
x	Characterization
x	Optimization

Background / Problem Statement

Evaluation results indicate that achieving the target package resistance requires a thin die. A die thickness of 4 mils was identified as necessary, but a die bond process for this configuration has not yet been established.

Objective Details

To identify significant factors affecting die bond output response using 4mils die thickness through characterization.
To optimize the identified factors affecting die bond output response from the characterization.

Variables Under Study

Dependent Variable/s (Response/s)	Continuous or Categorical?	Number of Replicates	Specification	Unit of Measurement
Bond Line Thickness	Continuous	1 (30 units/run)	1.0 - 2.5	mils
Tilt	Continuous	1 (30 units/run)	< 1.0	mils
Fillet Height	Continuous	1 (30 units/run)	25 - 75 (DT)	%
Epoxy Coverage	Continuous	1 (30 units/run)	> 75	%
Voids	Continuous	1 (30 units/run)	< 5	%

Independent Variable/s (Input Factor/s)	Continuous or Categorical?	Number of Factor Levels	Values of Factor Levels	Unit of Measurement
Dispense Pressure	Continuous	2	33 - 47	bar
Bond Force	Continuous	2	0.5 - 1.5	grams
Bond Delay	Continuous	2	75 - 100	ms

Experimental Design Used	**2 level Full Factorial**
# of Center Points Used	**2 Center Points**
Process/es Under Study	Die Bond
Equipment/s Used	ASM
Fixed Factors and their Levels Used	Dispense Z Height = 35
	Dispense Pattern Ratio = 100%
Assumptions & Limitations	The response modeing is limited to linear terms only due to resources limitation.

B. DOE Plan for Wire Bond Process

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Design of Experiment PLAN

Experimental Objective/s	
	Comparison
x	Characterization
x	Optimization

Background / Problem Statement

One challenge in assembly development is reducing overall package resistance to meet customer requirements. Evaluation results indicate that using a 2.5 mil Au PCC wire significantly lowers resistance, but a defined wire bond process for this wire size has not yet been established.

Objective Details

To identify significant factors affecting wire bond output response using 2.5 mil Au PCC wire through characterization.
To optimize the identified factors affecting wire bond output response from the characterization.

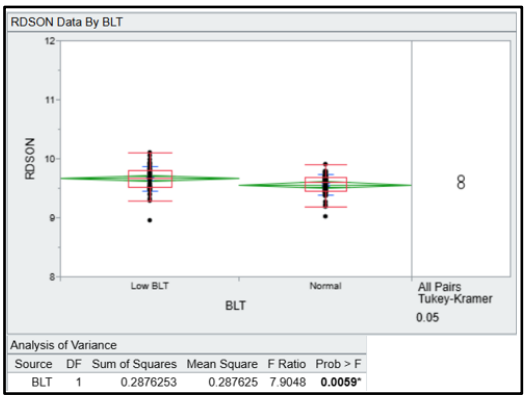
Variables Under Study

Dependent Variable/s (Response/s)	Continuous or Categorical?	Number of Replicates	Specification	Unit of Measurement
Ball Dimension	Continuous	1 (30 rdgs/run)	5.0 - 7.0	mils
Ball Thickness	Continuous	1 (30 rdgs/run)	1.0 - 2.0	mils
Intermetallic Coverage (IMC)	Continuous	1 (30 rdgs/run)	> 80	%
PMDr	Continuous	1 (30 rdgs/run)	20 - 40	%
Crater / Crack	Discrete	1 (30 pads/run)		-

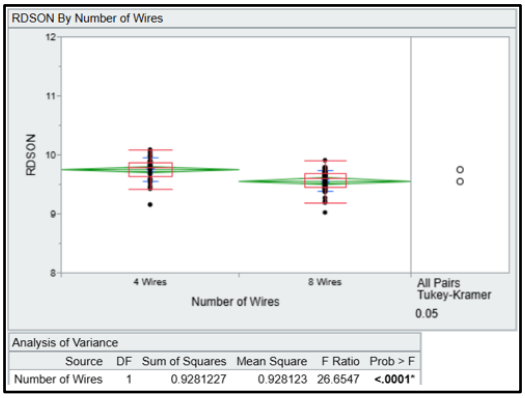
Independent Variable/s (Input Factor/s)	Continuous or Categorical?	Number of Factor Levels	Values of Factor Levels	Unit of Measurement
S2 US Power	Continuous	2	600 - 900	-
S2 Bond Force	Continuous	2	40 - 120	grams
S1 Bond Force	Continuous	2	300 - 700	grams

Experimental Design Used	**2 level Full Factorial**
# of Center Points Used	**2 Center Points**
Process/es Under Study	Wire bond
Equipment/s Used	SKW
Fixed Factors	Scrub Cycle and Scrub Cycle - 0
	Overall bond time - 27ms
Assumptions & Limitations	The response modeing is limited to linear terms only due to resources limitation.

C. RDSON vs. BLT



D. RDSON vs. Number of Wires



E. RDSON vs. Wire Supplier