ILASTIK: MACHINE LEARNING AI-BASED APPROACH FOR AUTOMATED QUANTIFICATION AND MINIMIZATION OF WIRE SWEEP INDUCED BY HIGH TG EMC IN LGA RF POWER PACKAGES

Marty Lorgino D. Pulutan
Jerome D. Amado

Backend Technologies
Ampleon Philippines, Inc., Light Industry & Science Park I, Brgy. Diezmo, Cabuyao City, Laguna
marty.lorgino.pulutan@ampleon.com

ABSTRACT

Among the critical challenges in overmolded Land Grid Array (LGA) Power Amplifier Module (PAM) packages is wire sweep—an encapsulation-induced deformation that compromises electrical reliability. The study investigated wire sweep behavior of LGA PAM which uses epoxy mold compound (EMCs) with high glass transition temperature (Tg) by employing a structured DMAIC methodology. Wire Sweep Index (WSI%) was quantified via developed macro program that uses AI-based machine learning ILASTIK software. Potential contributors were identified through Cause-and-Effect analysis and prioritized using FMEA. Measurement System Analysis (MSA) validated the reliability of WSI% quantification. A series of Plackett-Burman and Full Factorial DOE were conducted to isolate and optimize key parameters in both wirebonding and transfer molding processes. Results revealed that loop height, wire count and segmented transfer profiles significantly affect WSI% with optimized conditions reducing the rejection rate from 10.74% to 0%. Contour modeling and response surface analysis enabled the development of a design rule matrix (DRM) for future LGA PAM configuration.

1. 0 INTRODUCTION

The incessant advancement of mobile broadband technology along with the widespread integration of RF power devices across multiple industries has driven a surge in the demand for higher power which necessitates the use of EMCs with high-temperature stability in device packaging blueprint. A high Tg is then preferred, exceeding the operating junction temperature of the device. Maintaining a Tg above the junction temperature reduces the risk of CTE mismatch between the EMC and other critical package components particularly the EMC-pad interface. Moreover, selecting an EMC with excellent adhesion properties particularly to Cu and Ag-plated surfaces ensures stable mechanical bonding even under prolonged exposure to high temperatures and cyclic power loads. However, the continuous material property enhancement and modification of EMCs introduce mechanical challenges affecting device reliability. One of the most common defects induced especially by transfer molding during encapsulation is wire sweep. As the molten EMC flows and fills in the mold cavity, mechanical stress is applied to the fine bonding wires due to the drag force causing displacement from their intended positions. Excessive wire sweep can result in electrical short circuits and signal integrity degradation particularly in high-frequency and high-power applications. The extent of wire sweep is influenced by several factors including the rheology and flow characteristics of the EMC, wire material and diameter, wire loop height, and the molding process parameters.

Emerging low-stress EMC formulations with improved viscoelastic properties have shown promise in mitigating mechanical stress on wire bonds but industrial adoption remains limited due to product maturity. As power densities increase and semiconductor packaging advances toward miniaturization particularly in overmolded and LGA-type RF power packages, comprehensive wire sweep characterization and process co-optimization between wire bonding and molding are deemed essential.

Moreover, the current methodology employed at Ampleon for quantifying wire sweep involves manual annotation of X-ray images and calculation of the WSI% using Excel. Due to the labor-intensive and time-consuming nature of such approach, a sampling method is typically utilized instead of evaluating all wires across the dataset, which may limit the statistical representation and accuracy of the wire sweep assessment. This underscores the need for an automated, scalable, and objective method to analyze wire sweep across entire X-ray image datasets.

2. 0 REVIEW OF RELATED WORK

Per se, wire sweep is a common form of wire deformation characterized by the lateral displacement of the wire in response to the drag force exerted by the EMC flow. Such defects are governed by multiple factors including material characteristics, wire geometry, fluid dynamics, and process parameters. The wire sweep occurs when front flow

momentum causing drag force inflicted towards wires supersedes the sweep stiffness of the bonded wires as it flows through and fills up the entire mold cavity. Wire Sweep Index percentage is calculated using the formula:

$$Wire\ Sweep\ Index\ \%\ (WSI\%) = \frac{D_N}{L} \quad \text{(Equation 1)}$$

Where D_N is the maximum vertical projection of the deformation and deflection of the wire relative to initial position and L is the vertical projection length of wire before sweeping[1]. According to Lamb's model, the drag force experienced per unit length of wire is dependent on wire diameter, velocity, and the kinematic viscosity of the EMC material[1-3] which is given by:

$$D = \frac{1}{2}\rho U^2 dLC_D \quad \text{(Equation 2)}$$

For multiple wires, similar fluid properties are observed across adjacent locations when mold compound interference is neglected, leading to comparable sweep levels. However, due to fluid wake effects, drag force decreases for successive wires as upstream wires absorb initial momentum, resulting in reduced sweep for downstream wires near the mold gate[1, 4]. Consequently, dense wire layouts exhibit significantly lower WSI% compared to sparse configurations due to wake-induced drag reduction[3]. Narrow wire gaps further influence EMC flow by introducing localized resistance[5]. This phenomenon, termed the wire density effect, suggests that altered flow fields from one wire affect only adjacent downstream wires, modifying local drag force and sweep behavior[6].

Of all wire types, Au wires remain preferred in RF packaging for conductivity and corrosion resistance, yet larger diameters—though stiffer—are cost-prohibitive.[4, 7, 8] Instead, loop geometry is optimized where longer spans reduce sweep stiffness while shorter lengths with reduced loop heights and optimized kink placement enhance resistance.[7] Ali et al. confirmed wire length as the dominant wirebond parameter dictating WSI%[5] while orientation relative to EMC flow also pose a practical impact on sweep[9]. Leone et al. found that reduced loop height and wire length can keep WSI% below 10% with corner and perpendicular wires more susceptible[10].

Transfer molding parameters also significantly impact wire sweep. Mold flow turning at corners increases drag on adjacent wires[5]. Khor et al. attributed the high front flow momentum to the EMC cure kinetics at the package corners leading to turbulence[11]. Additionally, Ali et al. noted that corner wires with longer spans experienced higher sweep while preheat time, transfer and clamp pressures had limited influence. Leone et al. similarly highlighted the benefit of low-viscosity, long spiral flow EMCs[10, 12].

Minimizing WSI% relies on rheological tuning of EMC and process optimization. Studies advocate operating at low viscosity and long gelation times[10, 12, 13]. Hian et al. identified pellet preheat time, packing pressure, and transfer speed as significant mold parameters[14], while Liu et al. confirmed two-segment transfer modes and higher modulus Au wires lowered sweep[15]. Wu et al. emphasized tailoring parameters per EMC rheology[9].

Few works address simultaneous optimization of wirebond and mold parameters. Ali et al. showed that longer transfer time reduced sweep while other mold parameters had limited effect[12]. Of all published studies, only a few dealt with investigation on the relationship and interaction of mold process optimization with wire profile simultaneously in response to wire sweep.

.

3.0 METHODOLOGY

The initial phase of the methodology involved the development of an AI-based machine learning framework utilizing ILASTIK, integrated with Fiji, to enable automated measurement of WSI% from X-ray images. The implementation and structure of the custom Fiji macro program are detailed in Section 4.1.

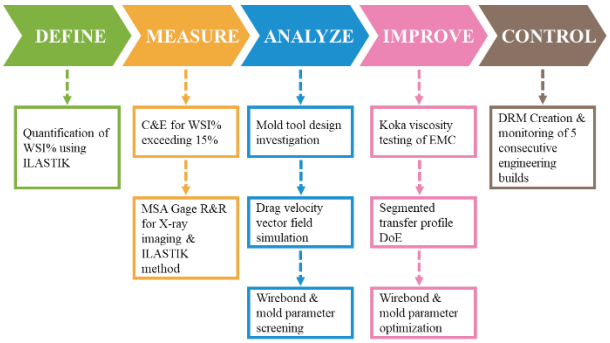

Fig. 1. DMAIC methodology applied to process optimization of wire sweep in LGA PAM packaging.

The second phase employed the DMAIC methodology, as illustrated in Fig. 1. The study utilized a high Tg EMC and Au wire in an actual GaN die assembly, following a standard process flow for LGA PAM packaging.

4.0 RESULTS AND DISCUSSION

4.1 Development of Macro Program for Automated WSI% Calculation Using ILASTIK

X-ray image analysis of Au wires was conducted using ILASTIK, an open-source machine learning-based segmentation platform. The software enabled effective pixel-wise classification, isolating Au wires from the background

with high accuracy. All X-ray images were organized in a designated directory to facilitate streamlined batch processing within ILASTIK.

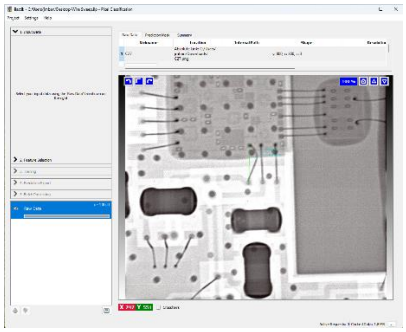

Fig. 2. ILASTIK GUI showing representative X-ray image to be used for recipe creation.

Using pixel classification, a representative X-ray image was loaded into ILASTIK to develop a classifier recipe. Feature selection was employed to enhance wire detection by leveraging differences in intensity, edge contrast, texture, shape, and local neighborhood patterns. Manual annotations were applied to distinguish Au wires from surrounding components, enabling the software to learn and accurately differentiate the subject from background. Successful segmentation yielded classified images in which Au wires were highlighted in blue while non-target regions were marked in yellow (see Fig. 14 in Appendix). The resulting predictions were exported in HDF5 format to a designated directory accessible by Fiji. A custom macro was developed in Fiji to batch process the classified HDF5 files. Upon loading, the images were denoised following skeletonization to eliminate residual artifacts that could compromise the accuracy of WSI% computation. The macro was programmed to automatically calculate WSI% based on Equation 1.

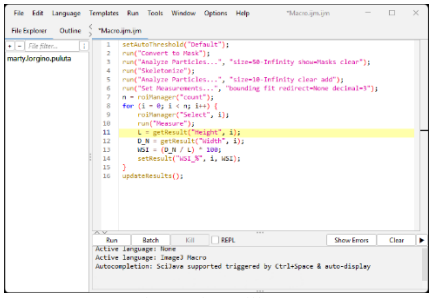

Fig. 3. Macro Program Creation Using Fiji Macro Language.

To validate the applicability of the trained classifier across all X-ray images, the remaining images were batch processed using the established prediction mask. The segmented outputs were overlaid and compared with the original X-ray images to verify that all Au wires were accurately captured. Upon confirmation, the Fiji macro was deployed for automated, simultaneous processing. The computed WSI% values were displayed in the Fiji Results dialog box.

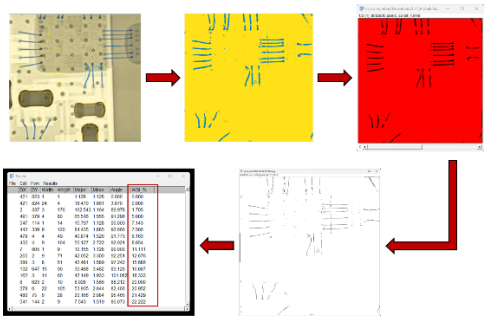

Fig. 4. Automated WSI% Calculation Routing Using ILASTIK and Fiji.

The automated WSI% analysis workflow consists of two primary steps: (1) launching the ILASTIK interface and loading all X-ray images using the pre-trained classifier recipe, and (2) executing the dedicated macro program in Fiji for WSI% computation. The total processing time is dependent on the number of images analyzed; a trial run involving 10 X-ray images completed in approximately 1 minute and 25 seconds.

4.2 Define: Quantifying Wire Sweep Index and Current Yield Performance Post Mold in LGA PAM

The actual WSI% for three consecutive engineering builds were measured and quantified through ILASTIK.

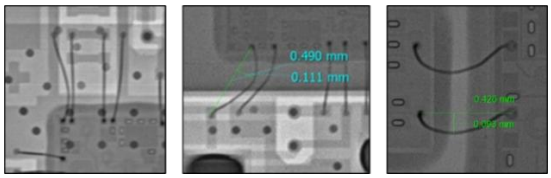

Fig. 5. X-Ray Images of LGA PAM Device Units with Observed Wire Sweep Post Mold Cure.

WSI% were measured on all detected wires in the X-ray images. On average, 310 wires across the three engineering builds exhibited wire sweep as presented in Fig. 6.

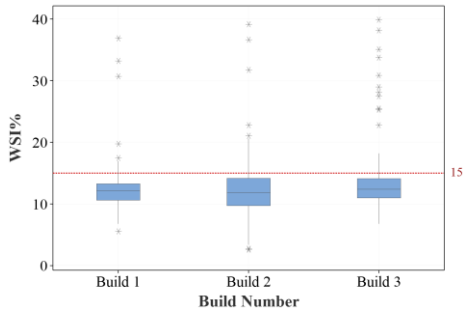

Fig. 6. Distribution of WSI% of Wires From Three Consecutive Engineering Builds.

Based on the predefined maximum wire sweep criterion of 15%, a portion of the upper whisker and extreme outliers exceeding the upper fence (Q3 + 1.5IQR) were observed. The

measured maximum wire sweep reached up to 39.63% with an average defect rate of 10.74% across all three engineering builds which impacted the overall yield of functional samples. Unacceptable and anomalous yield indicates underlying causes of wire sweep, underscoring the need for further process or material optimization.

4.3 Measure: Identifying Possible Contributors and the Root Cause of Wire Sweep in LGA PAM

From the LGA PAM process flow, problem-solving focused on wirebonding, backend molding, and related materials. A Cause & Effect (C&E) Analysis identified 24 potential factors contributing to WSI% >15%. These were evaluated using a C&E Matrix based on relevance to WSI%, yield, reliability, and test performance. Seven key factors out of 24 were selected for risk assessment.

Gage R&R was conducted to evaluate the consistency of WSI% measurement using ILASTIK post-PMC. Results showed 99.96% of variation was due to part-to-part differences, indicating high measurement repeatability and reproducibility across operators and methods (X-ray and ILASTIK). Control charts confirmed stability, and ANOVA showed no significant variation from operator ($p = 0.643$) or method ($p = 0.466$). Thus, ILASTIK was chosen for WSI% quantification.

4.4 Analyze: Risk Analysis and Validation of Potential Critical Factors to WSI% Exceeding 15%

Out of the 7 potential critical X's identified from C&E, only 4 obtained high RPN and would proceed for on-off validation.

Table 1. Identified potential critical factors and respective impact to WSI% in LGA PAM.

No.	Process	Potential Critical Factor	Impact
1	Machine	Mold tool design issue	5%
2	Material	Design requirements	15%
3	Wirebond	Unoptimized wirebond parameters	40%
4	Mold	Unoptimized molding parameters	40%

4.4.1 Critical Factor No. 1: Effect of Mold Tool Designs

Short-shot molding at 50% was conducted on bare LGA PAM strip to check uniformity of mold flow from cavity. In parallel, transfer mold flow simulation was done to verify the theoretical mold flow behavior across the strips using actual measured dimensions of the tool. From the strip mapping of units with deflected wires, an apparent localization was observed which coincides with the projected non-uniform flow of EMC on the upper and lower strip (as referenced to Fig. 7 below) wherein the upper strip indicates faster flow based on larger area of coverage. Moreover, indications of jetting or sudden surge of EMC transfer flow are observed on some portions of the cured short-shot EMC. The influence of mold tool design was then evaluated by comparing the newly fabricated and the previously employed tool performance.

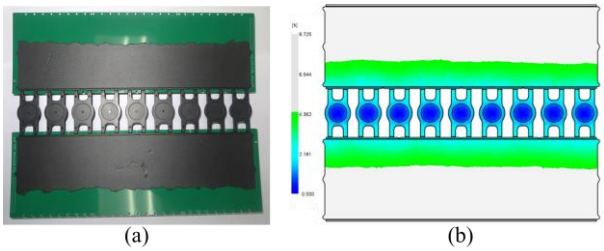

Fig. 7. Comparison of (a) Actual Short-Shot Molding Strip and (b) Simulated Flow Front Profile.

The paired t-test comparing the randomly sampled 50 deflected wires from units molded under tool A (newly fabricated) and tool B (previously employed tool in the same machine) showed significant difference (p-value = 0.000) indicating that utilization of tool A has contributed to the increase in WSI% of the wires post mold (see Fig. 17 in Appendix). The gate dimensions A, B, C, and D in the right and left cavity of tool A were measured and compared.

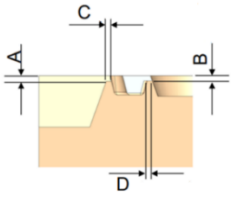

Fig. 8. Gate Dimensions in the Right and Left Cavity of Tool A.

A significant difference of 0.034mm was noted between the 1st gate depth (dimension A) of left and right cavity which might have triggered the imbalance and surging of mold flow along the left cavity. The tool was then reworked to reduce the difference to about 0.002mm and the wire sweep performance was then reassessed and compared with tool B.

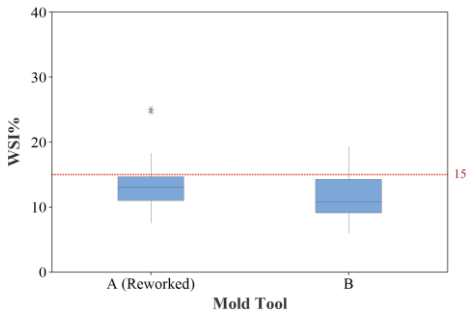

Fig. 9. Comparison of WSI% of Device Units Molded Using Reworked Tool A and Tool B.

Using the same statistical test, no significant difference (p-value = 0.021) is observed between the WSI% measured on units molded using the reworked tool A compared to tool B. The WSI% was decreased to an average of 11.550% and the number of wire sweep rejects whose WSI% is more than 15% criterion reduced to 7.03%. However, the 7.03% rejection rate implies that there are other underlying critical factors contributing to the occurrence of high WSI%.

4.4.2 Critical Factor No. 2: Restrictions of product design complexity and requirements

While a larger-diameter Au wire is generally preferred for enhanced reliability,[4, 7, 8] a 38-µm wire diameter was instead selected and utilized to achieve a balanced trade-off with cost. Computational simulations were conducted to analyze the drag velocities of the high Tg EMC's front flow momentum during transfer molding to identify regions with high turbulence formation. Such zones with high turbulence were correlated with areas in the package layout where wire deflection was more prevalent.

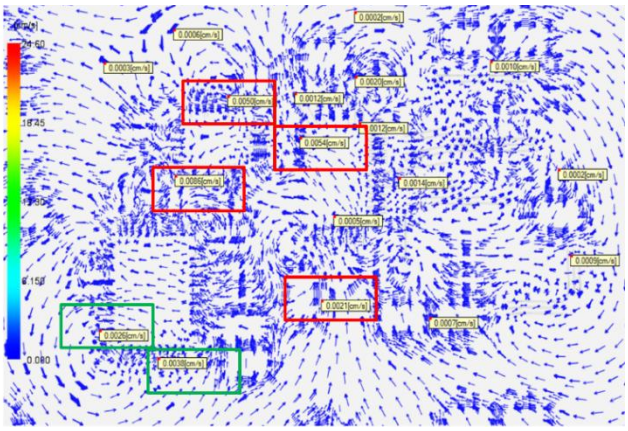

Fig. 10. Simulated Drag Velocity Vector Field During Transfer Molding of High Tg EMC on LGA PAM.

The red-framed zones exhibited significantly higher drag velocities compared to other regions which highly correlated with areas characterized by a high incidence of wire deflections with values exceeding 15%. In contrast, the green-framed zones demonstrated drag velocities comparable to those observed in the red-framed zones but did not show evidence of wire deflections with WSI% exceeding 15% highly attributed to the low loop and short wire span of wires bonded on the lone controller die bonded on this region[1-3].

To evaluate the influence of product design complexity and requirements on the wire sweep defect rate and percentage, LGA PAM was compared to a non-PAM LGA package with identical package outline dimensions. The latter package, however, utilized a different EMC grade, a less complex die layout configuration, a lower loop height, a shorter wire span, and fewer wires.

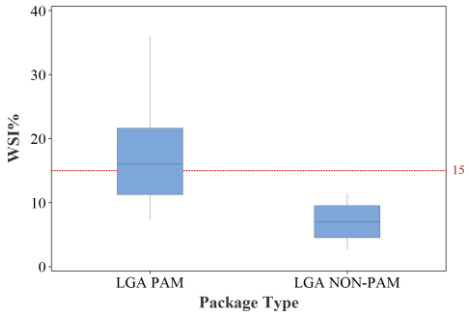

Fig. 11. Comparison of WSI% of LGA PAM and Non-PAM Device Units.

The WSI% of the LGA Non-PAM package was observed to be significantly lower compared to the LGA PAM configuration with 53.33% of the LGA PAM data exceeding the upper specification limit and reaching a maximum WSI% of 35.02%. The discrepancy is primarily attributed to the inherent differences in package design complexity as the LGA PAM variant requires denser and more intricate layout coupled with the use of low spiral flow EMC, which cannot be modified further due to application-specific constraints. Consequently, to mitigate wire sweep and maintain WSI% within specification thresholds, process optimization should focus on fine-tuning wirebond and molding parameters.

4.4.3 Critical Factor No. 3: Screening out significant factors in wirebond process

A Plackett-Burman Screening DOE approach was employed to identify the statistically significant factors among the wirebond parameters influencing wire sweep behavior. The parameters investigated included the number of wires, loop height, wire pitch, wire span, wire diameter, and wire angle relative to the mold gate. Each factor was evaluated at two levels, corresponding to the extreme values observed within the current LGA PAM design configuration ensuring that the design space adequately represented the operational bounds of the existing process.

Table 2. Wirebond Parameters and Levels for PBD Screening DOE Matrix.

Parameter	Factor Levels
No. of Wires	1, 10
Loop Height (µm)	700, 1500
Wire Pitch (µm)	200, 4000
Wire Span (µm)	1500, 3000
Wire Diameter (µm)	20, 50
Wire Angle (degrees)	0, 90

Results revealed that all investigated wirebond parameters exhibited p-values less than 0.05 except for wire angle, indicating that the wire's orientation relative to the mold gate

does not significantly influence WSI% as opposed to earlier reports[5] possibly due to dense and complex die layout of the device. Moreover, values of the adjusted SS highlights wire diameter as the most influential factor accounting for 36.62% of the total variation in WSI% due to increased geometric dimensions which consequently increases sweep stiffness[1-4]. It is followed by loop height (22.40%), number of wires (21.73%), and wire span (13.59%) known to reduce sweep stiffness[7]. Conversely, wire pitch demonstrated a relatively minor effect on WSI% based on adj MS unlike previous studies reported[3-5] even if the interval between the two levels are large, as it is nested under the number of wires which is a constraint imposed by the design architecture of the LGA PAM package. The design adhered on using smaller wire diameter for cost reduction. All other significant wirebond parameters will be optimized alongside with significant mold parameters screened on the next section.

4.4.4 Critical Factor No. 4: Screening out significant factors in transfer molding process

Similar Screening DOE approach was used to identify the statistically significant factors among the transfer molding parameters influencing wire sweep behavior. The parameters investigated are as shown in Table 3, each at two levels using the pre-selected high Tg EMC.

Table 3. Transfer Molding Parameters and Levels for PBD Screening DOE Matrix.

Parameter	Factor Levels
Transfer Time (s)	8, 15
Pellet Pre-Heat Time (s)	3, 5
Cure End Pressure	70, 90

Results showed that only transfer time exhibited a statistically significant effect on WSI% (p-value = 0.002). In contrast, pre-heat time and cure end pressure were determined to be non-significant, demonstrating minimal impact on WSI% based on low adjusted SS and MS values as opposed to the results obtained by Hian et al.[14] but agrees well with Ali et al.[12]. The results may be possibly due to wire sweep occurrence at EMC flow-front propagation and not during packing stage, while pre-heat conditions may not possibly affect the Koka viscosity of the EMC. Further optimization will focus on refining the transfer profile, considering the total transfer time along with its potential interactions with the identified significant wirebond parameters.

4.5 Improve: Effect of segmented transfer profile, pre-sway and optimized wirebond on WSI%

The Koka viscosity plot of low spiral flow EMC material as shown in Fig. 12, suggests operating zone for mold transfer should be within 5 to 6 seconds as opposed to current transfer time of 15 seconds where EMC already loses its ability to flow and thus increases its drag force and front flow momentum rapidly[10, 12, 13].

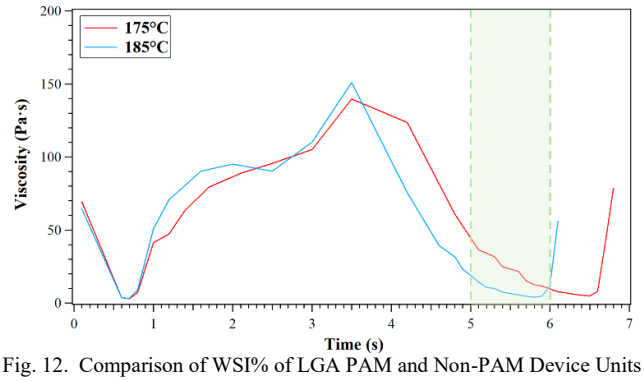

Fig. 12. Comparison of WSI% of LGA PAM and Non-PAM Device Units

Based from the koka viscosity plot, straight and segmented transfer profiles were derived based on cumulative recommended operating window as shown in Table 4.

Table 4. Straight and Segmented Transfer Profiles Derived from the Koka Viscosity Plot of the High Tg EMC.

Leg No.	Profile	Time (s) (1st Segment)	Time (s) (2nd Segment)
1	Straight	5	
2	Straight	6	
3	Segmented	2	3
4	Segmented	1	4
5	Segmented	2	4
6	Segmented	1	5

In the segmented transfer profile, the 1st segment transfer time is deliberately maintained at a shorter duration relative to the second segment as the latter requires an extended time to ensure complete cavity fill. A General Full Factorial DOE was conducted to evaluate the influence of transfer profile parameters on WSI%. The results indicate that the type of transfer profile exerts a statistically significant effect on WSI% (p-value = 0.021). The implementation of a segmented transfer profile resulted in an estimated WSI% reduction of 6.77% based on the estimated mean difference. Furthermore, increasing the 1st segment transfer time from 1 second to 2 seconds yielded an additional 3.09% reduction in WSI%, a difference statistically supported by both Tukey's HSD and Fisher's LSD post-hoc pairwise comparisons. Lastly, the cumulative transfer time of 5 to 6 seconds of the segmented transfer profile yielded a p-value of 0.052 suggesting a marginally non-significant effect on WSI%. The evident effect of segmented transfer profile in agreement with the lowest koka viscosity point agrees with the findings of Hian

et. al and Liu et al.[14, 15]. While the result does not meet the conventional threshold for statistical significance, such indicates a potential influence that could be further investigated along with wirebond parameters and potential interactions.

An extensive Full Factorial General DOE with varying levels per factor while accounting for the restrictions of LGA PAM design footprint, was conducted to determine optimum wirebond and mold parameter combinations. Results to be used as input for DRM of LGA PAM architecture considering the risk and mitigation of wire sweep.

Table 5. Combined Significant Factors in Wirebond and Mold Influencing WSI%.

Parameter	Factor Levels
No. of Wires	1, 15, 30
Loop Height (µm)	700, 1100, 1500
Wire Span (µm)	1500, 3000
Transfer Profile	A, B
Pre-Sway (%)	0, 5

In the matrix presented above, Transfer Profile A and B represent legs 3 and 5 in Table 4 respectively. The coefficient of determination (R^2) is approximately 93.68%, indicating a high level of explanatory power in the model. The number of wires and loop height emerged as the most influential factors affecting WSI% with p-values of 0.0035 and 0.010 respectively. The high impact of loop height agrees with the findings of Leone et al. that shorter loop height decreases susceptibility to wire sweep[10] while number of wires is attributed to the decreased wire pitch due to wire density effect[6]. A contour plot was then subsequently generated utilizing the two most significant variables, with the number of wires plotted on the x-axis given its predominant impact on WSI% as determined by the adjusted SS and MS.

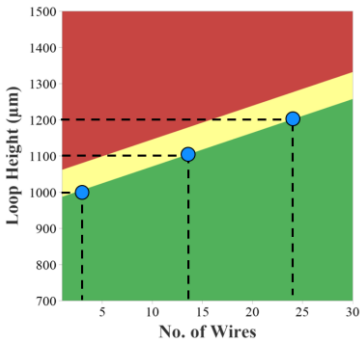

Fig. 13. Contour Plot of Predicted WSI% per Loop Height and No. of Wires at 0% Pre-Sway Configuration.

The hold values for the contour plot as shown in Fig 13 are 1500 µm wire span, transfer profile A and no pre-sway. The plot suggests that wire loop height more than 1300 µm at any combination of wire number falls within the red zone which highly likely to yield wire sweep more than 15%. A leeway of approximately 15 to 25 wires would make 1200 µm fall within yellow zone whose wire sweep is between 10 to 15 µm, a risk zone in case maximum WSI% is tightened to at most 10 µm. Thus, designs should constrain loop height to ≤1200 µm with ≥25 wires per group. For single-wire configurations, the maximum viable loop height is 1000 µm.

With 5% pre-sway applied, a 1300 µm loop height becomes feasible with ≥25 wires per group, and single-wire configurations are viable up to 1100 µm (see Fig. 18 in Appendix). Response optimization identified the optimal setup—30 wires, 700 µm loop height, 1500 µm span, Transfer Profile A, and 5% pre-sway—yielding a composite desirability of 1.0 at target WSI% = 0%. While the primary goal was to keep WSI% below the USL of 15%, feasible parameter ranges were derived from overlaid contour plots (Table 6).

Table 6. Minimum Number of Wires Required per Loop Height With and Without Pre-Sway.

Loop Height (µm)	Minimum No. of Wires	
	0% Pre-Sway	5% Pre-Sway
≤ 900	No Minimum	No Minimum
1000	2	No Minimum
1100	13	2
1200	24	14
1300	> 30	24

4.6 Control: DRM Creation and Monitoring of WSI% Performance

Based on the findings from the optimized wirebond and mold configurations, a DRM was established and disseminated to design teams to enforce constraints particularly on wirebond layouts to mitigate WSI%. The final layout incorporating adjusted wire configurations, was implemented in subsequent builds during which the WSI% ≥ 15% rejection rate was tracked over five consecutive runs (see Fig. 19 in Appendix). Following deployment of the DRM and utilization of the optimized transfer mold profile, wire sweep-related rejects were fully eliminated.

5.0 CONCLUSION

The study successfully identified the factors inducing WSI% exceeding 15% in LGA PAM packages through a structured DMAIC approach. Root cause analysis identified four critical

factors: mold tool design, product design complexity, unoptimized wirebond parameters, and transfer molding settings—determined through statistical screening and simulation. Subsequent optimization, including mold tool rework, implementation of segmented transfer profiles, and adjustment of wirebond configurations, resulted in significant reductions in WSI%. A series of DOE confirmed that wire count and loop height were the factors with the highest impact on WSI%, with a validated parameter set achieving optimal wire sweep control. Additionally, AI-based machine learning using ILASTIK was successfully implemented to achieve 100% measurement of WSI% on all wires, replacing conventional sampling and providing a more comprehensive and reliable dataset. The findings provide a data-driven foundation for establishing design rules and process windows that minimize wire sweep risk while accommodating the electrical and mechanical requirements of the LGA PAM package.

6.0 RECOMMENDATIONS

To further improve the study, the researchers recommend establishing workable parameter windows for smaller Au wire diameters such as 20 µm, to be incorporated into the DRM. Additionally, EMCs exhibiting varying spiral flow characteristics should be evaluated to develop a predictive model correlating spiral flow behavior with WSI% in response to wirebond and molding parameters. Finally, it is noteworthy to investigate the influence of different die thicknesses and layout configurations on the front flow dynamics of the EMC as such factors may significantly impact wire sweep performance.

7.0 ACKNOWLEDGMENT

The authors wish to extend their deepest appreciation to the engineers and technicians at the Backend Technologies Competence Center for their assistance in conducting the experiments, to Failure Analysis & Reliability Department for the execution and provision of necessary tools, tests and support in the experiment, and to the management team of Ampleon Phils. Inc. for their support, which was instrumental in facilitating this research.

8.0 REFERENCES

1. M. R. Marks et al., ***IEEE Trans. Compon. Packag. Manuf. Technol.***, *4(12).* **2014**. 2042-2057.
2. J. Han et al., ***13th EPTC***, **2011**. 667-673.
3. H. Chai, Y. Zohar, ***J. Electron. Packag***., *121*, **1999**, 137-142.
4. S. Huang et al., ***71st ECTC***, **2021**. 1464-1468.
5. S. S. S. Ali, et al., ***Int. J. Precis. Eng. Manuf***., *15*, **2014**, 1793-1799.
6. C. C. Pei et al., ***8th ISAPM***, **2002**. 160-165.
7. H. Kung et al., ***Microelectron. Eng.***, *85(9)*, **2008**, 1902-1909.
8. H. S. Chen et al., ***ICEMP***, **2009**. 204-207.
9. H. Wu et al., ***25th ICEPT***, **2024**. 1-6.
10. F. Leone et al., ***25th EPTC***, **2023**. 635-641.
11. C. Y. Khor et al., ***Int. J. Heat Mass Transf***., *54*, **2011**, 1861-1870.
12. S. S. S. Ali et al., ***24th EPTC***, **2022**. 5-10.
13. L. Nguyen et al., ***47th ECTC***, **1997**. 60-71.
14. S. T. S. Hian et al., ***13th EPTC***, **2011**. 764-768.
15. J. M. Liu et al., ***9th EPTC***, **2007**. 61-65.

9.0 ABOUT THE AUTHORS

Marty Lorgino D. Pulutan received the B. S. degree in Applied Physics specializing in Materials Physics from University of the Philippines, Los Baños in 2017 and currently pursuing M. S. degree in Materials Science and Engineering by Research in Mapua University. He has published a total of 10 papers in peer-reviewed journals and international conference proceedings. He is currently a Senior Materials Development Engineer under Back End Technologies Department in Ampleon Philippines, Inc.

Jerome Amado received his B.S. degree in Electronics and Communications Engineering from Adamson University, Manila. He is currently a Principal Engineer – Project Management under Back End Technologies Department in Ampleon Philippines Inc.

10.0 APPENDIX

Fig. 14. Segmented Imge Classified Through ILASTIK.

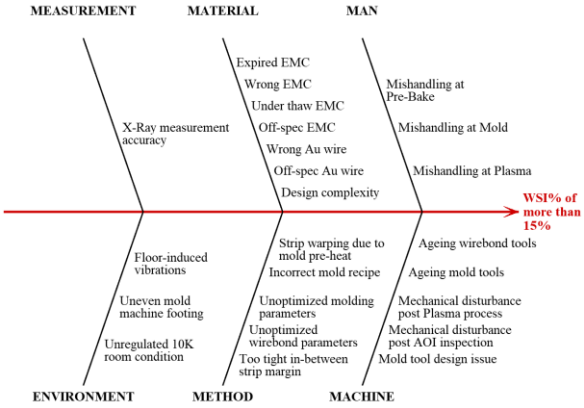

Fig. 15. Fishbone Diagram of All Potential Root Causes to WSI% Exceeding 15%.

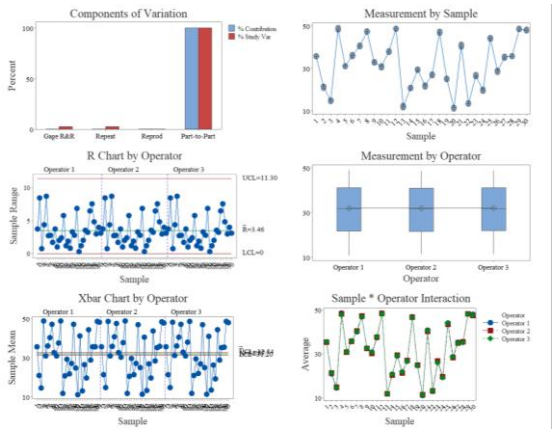

Fig. 16. MSA Gage R&R for WSI% Measurement Using X-Ray and Fiji Post-Processing.

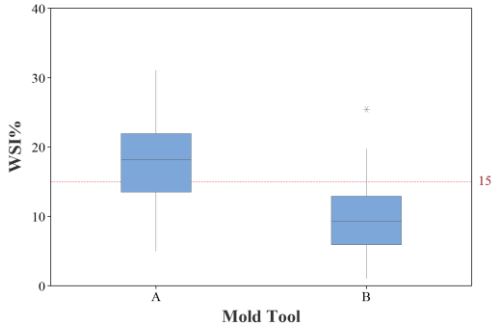

Fig. 17. Comparison of WSI% of Device Units Molded Using Tool A and Tool B.

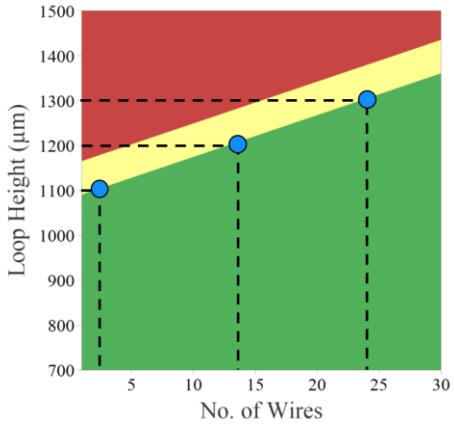

Fig. 18 Contour Plot of Predicted WSI% per Loop Height and No. of Wires at 5% Pre-Sway Configuration.

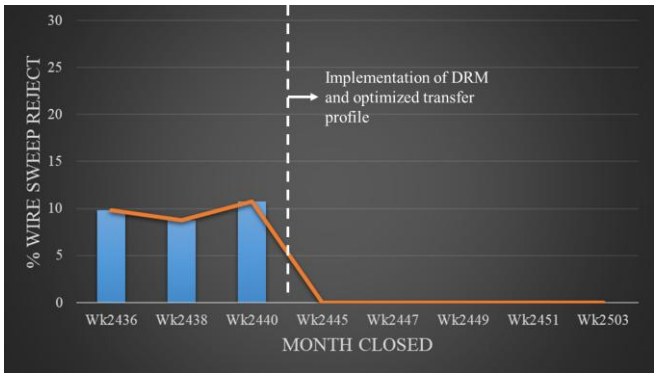

Fig. 19. Trend of Wire Sweep Reject Rates Before and After Implementation of DRM and Optimized Transfer Profile. A significant reduction to 0% wire sweep rejection was achieved from Week 2445 onward, indicating the effectiveness of the corrective actions.