A SPLIT-SITE TESTING APPROACH TO MINIMIZE CROSS-TALK-INDUCED EEPROM PARAMETER FAILURES

Aldrin D. Urriza
Leslie-Pearl L. Carada
Joshua Yvan S. Yray

Operations Test Engineering
ams-OSRAM, No. 2 Makiling Drive, Carmelray Industrial Park II, Barangay Milagrosa Calamba, Laguna
aldrin.urriza@ams-osram.com / leslie-pearl.carada@ams-osram.com / joshua.yray@ams-osram.com

ABSTRACT

During high-parallel EEPROM endurance testing, unexplained early-cycle failures emerged at a specific test site using newly qualified hardware despite 100% pass rates across all functional, parametric, and stress stages. The affected site yielded 0% during the first program/erase (P/E) loop, while legacy hardware consistently sustained >98% yield. To address this urgent issue, a DMAIC-based diagnostic approach was deployed, encompassing test program isolation, split-site grouping, hardware cross-swapping, and per-site data correlation.

Root cause analysis revealed that using the newer probecards are with possible latent defects within the PCB structure that triggered interferences at the site level, causing consistent readback errors and inaccurate loop count tracking. A masked pass condition in the first-read test further delayed detection. Implementing split-site strategies (e.g., sites 1–8 vs. 9–16) significantly reduced the failure rate and restored the affected site's performance to >95% yield in isolated configurations.

This paper presents a structured failure analysis, highlights the importance of site-level diagnostics in multi-site test environments, and proposes procedural improvements for enhancing test robustness during hardware transition and high-parallel test execution.

1. 0 INTRODUCTION

Endurance testing plays a critical role in validating the reliability of EEPROM devices under repeated program/erase conditions. In high-parallelism production environments, detecting marginal failures becomes increasingly difficult due to the interferences among active sites and test instrumentation. A recent escalation in yield loss isolated to a specific test condition necessitated a structured investigation to isolate failure mechanisms and mitigate production impact.

This section outlines the technical context, identifies the key test setup characteristics, and describes the observed anomalies that prompted deeper investigation.

1.1 Probecards in Wafer-Level Testing

Probecards serve as electrical interface tools between test equipment and semiconductor wafers during wafer-level testing, especially at the pre-bump sort stage. These tools enable precise signal delivery and measurement for various test categories including functional, parametric, and reliability screening such as endurance.

1.1.1 Probecard Qualification and Deployment

The newly qualified probecards underwent verification during the second wafersort stage testing, which focuses on parametric and functional checks following initial stress. First-stage endurance test focuses mainly on pass/fail outcomes under stress, so the new probecards had not yet undergone the in-depth parametric and functional evaluations that occur in later test phases. As a result, certain site-specific behaviors only became apparent during early production use. This outcome highlighted the added value of aligning test coverage with the specific demands of each qualification stage, particularly for endurance-sensitive operations.

1.2 EEPROM Reliability and Endurance Testing

Electrically Erasable Programmable Read-Only Memory (EEPROM) endurance testing serves as a fundamental reliability screening process in non-volatile memory validation. It involves subjecting memory cells to repeated Program/Erase (P/E) cycles to detect marginal behavior, degradation, or outright failure under stress. This test step is typically performed at wafer-level production to guarantee product longevity and specification compliance.

1.2.1 Endurance Cycle Mechanism

Each endurance cycle consists of two core operations: a Program phase where charge is injected into memory cells to write data, and an Erase phase where the stored charge is removed to reset the cell. These operations stress the oxide and floating gate structures, gradually degrading cell integrity over time.

1.2.2 Test Objectives and Failure Modes

The objective of endurance testing is to verify the memory's ability to withstand a defined number of P/E cycles (typically >10k) without functional loss. Common failure modes include bit retention loss, threshold voltage shift, and marginal readback values that indicate charge leakage or incomplete switching.

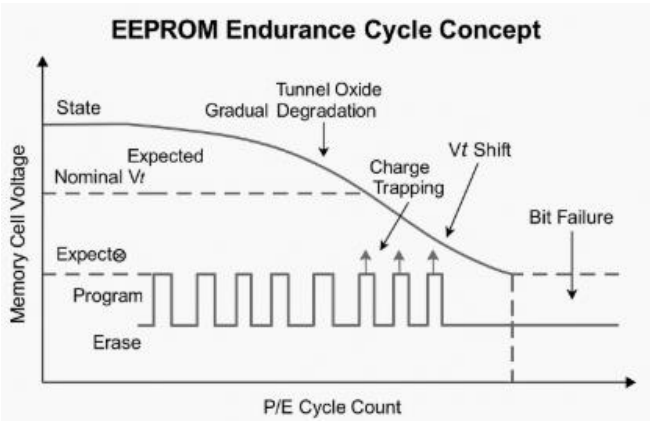

Fig.1. Conceptual diagram of the EEPROM endurance test cycle, showing repeated program/erase (P/E) operations used to evaluate memory cell reliability under stress.

1.3 Test Environment and Site-Level Configuration

Modern production environments utilize high-parallelism wafer probing systems to maximize throughput. Tests are executed across multiple sites, applying simultaneous stimuli to device under test. While this enhances efficiency, it can introduce site interferences that may mask or exaggerate marginal test behaviors.

1.4 Early Test Assumption Error

The endurance test framework relied on a simplified assumption for validating the outcome of the first program/erase (P/E) cycle. This assumption masked early test failures by enforcing a fixed pass condition, which ultimately delayed the discovery of genuine readback issues and led to incorrect loop count logging. A deeper look into this misconfiguration revealed how early-cycle behavior could evade detection under static test logic.

1.4.1 Static Read Expectation Design

The endurance test initially incorporated a static expectation for the initial read operation configured to always pass with a fixed return value. While this approach can simplify validation under normal conditions, it posed a significant diagnostic blind spot when true device behavior deviated early in the endurance loop.

1.4.2 Impact on Failure Detection and Yield Reporting

Because the test did not dynamically evaluate actual readback values during the first P/E cycle, the presence of invalid memory states—such as values like 41h or 592h—went undetected. As a result, the system incorrectly logged these failures as successful completions, causing premature termination of the endurance sequence (e.g., recording EnduranceLoopCount = 1 instead of the intended pass criteria).

2. 0 REVIEW OF RELATED WORK

Not Applicable.

3.0 METHODOLOGY

3.1 Define Phase

A production-critical yield issue emerged during EEPROM endurance testing, where newly qualified probecards caused a 0% pass rate at a specific site. The goal of this project is to identify and eliminate the root cause of these anomalous early-cycle failures to enable full deployment of the new hardware in high-parallel test environments.

Due to the failure's immediate impact on throughput and device qualification, a structured DMAIC-based problem-solving methodology was initiated to recover yield, ensure hardware stability, and sustain production output under strict delivery timelines.

3.2 Measure Phase

The process flow, current performance metrics, and data variability were systematically visualized to identify critical areas of deviation, serving as a foundational input for the subsequent Analyze phase.

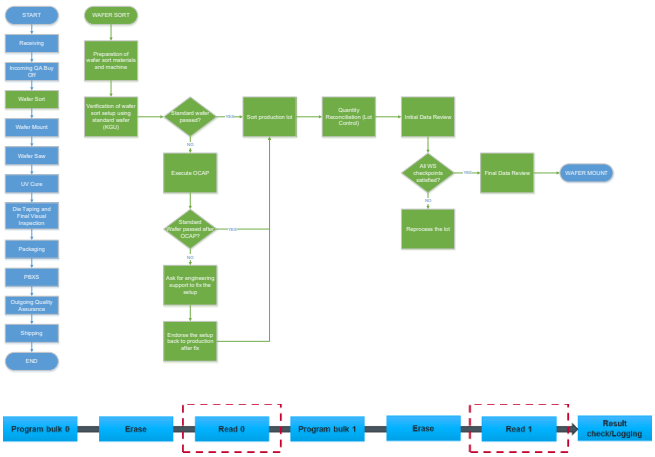

Fig.2. Process mapping for wafer sort including the conceptual procedure of the Endurance loop count test.

A pronounced spike in failure rate was observed at one test site (site 10) during the Endurance Loop Count evaluation, contributing to a significant yield reduction to 91% on a single wafer, as illustrated in Fig. 3. Notably, this site-specific anomaly was exclusive to the newly introduced probecards and was not replicated on legacy hardware.

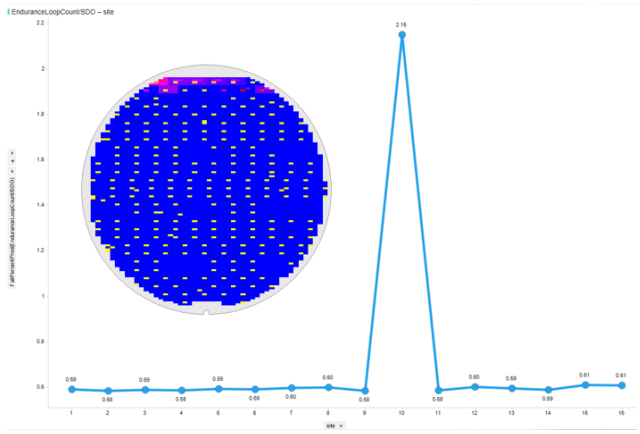

Fig.3. Showing the failure rate of one test site and the statistics indicating the average yield below the intended target.

3.3 Analyze Phase

Ishikawa diagram as shown on Fig.4 was used to show all the potential factors along with the tabular assessment and ranking for prioritization as shown in Fig.5.

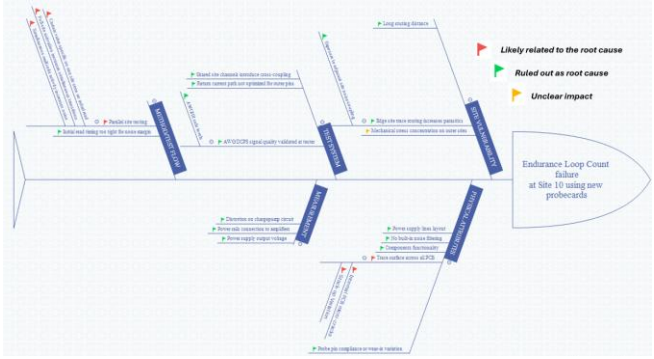

Fig.4. Ishikawa Diagram including Method, Test System, Site Variability, Physical Attributes and Measure

Category	Potential Root Cause	Analysis of Root Causes	Rank
Site Vulnerability	Mechanical stress concentration on outer sites	Hypothesized due to edge position but unproven by metrology. No significant difference from other probe cards.	Non-Factor
	Long routing distance	Logical assumption from layout position but needs measurement or simulation to quantify. No significant difference from other probe cards.	Non-Factor
Test System	Shared site channels introduce cross-coupling	Test pins used different channels.	Non-Factor
	Return current path not optimized for outer pins	Underlying PCB topology may favor central return paths. No issue seen on pin-to-pin checks.	Non-Factor
	AWG signal quality validated at tester	Tester outputs verified and proven stable. No contribution from equipment side.	Non-Factor
Method/Test Flow	Parallel site testing	Confirmed condition under which failures occur. Failures disappear in split-site testing, validating noise coupling as a trigger.	Factor
	Initial read timing too tight for noise margin	Additional delays or wait times do not have significant effect to the test itself.	Non-Factor
Measurement	Distortion on charge-pump circuit	Confirmed no issue on the output during bench testing.	Non-Factor
	Power rails connection to amplifiers	Done checks and replacement of LM317 and capacitors but failure is still manifesting.	Non-Factor
Physical Attributes	Layout and Design	No significant differences on the design and layout that will highly affect the test parameter in question confirmed with the Design Engineer.	Non-Factor
	Internal PCB traces	Internal PCB traces with possible micro-crack can disrupt signal integrity.	Factor

Fig.5. Assessment of potential root causes showing the ranking and expert's assessment

The potential factors were individually verified according to their ranking and prioritization and 16 factors were reduced to 2 potential factors related to the test methodology and physical attributes.

Method

X_1 Parallel Site testing - The existing test methodology utilizes parallel (full-site) testing to maximize throughput by activating all test sites simultaneously. While efficient, this mode introduces a high degree of concurrent switching activity, which can elevate the system's electrical noise floor and increase the risk of signal coupling between adjacent sites.

$X_{1.1}$ Abnormal early readout

$X_{1.2}$ Full site activation

Physical Attributes

X_2 Internal PCB traces - The possibility of latent defects within the internal PCB structure must be considered. Microcracks in internal copper traces, often caused by mechanical stress during probing, or PCB warpage, can lead to intermittent signal integrity issues or localized resistance increases. These faults may not always manifest under static test conditions but can become evident during dynamic or endurance testing.

$X_{2.1}$ Micro-cracks and Stack-up Variation

Subsequent analysis shows the method and results of the validation for the 2 potential factors and its subfactors.

3.3.1 Abnormal Early Readout

During failure analysis, it was observed that Site 10 exhibits a readout response even during the first test loop as seen in Fig.6, immediately after the endurance stress. This behavior is unexpected, as read operations are not expected to trigger or return valid data at that stage. The presence of a premature or abnormal readback on Site 10 suggests that the signal path is being influenced, likely due to crosstalk or unintended coupling from neighboring sites during full-site activation.

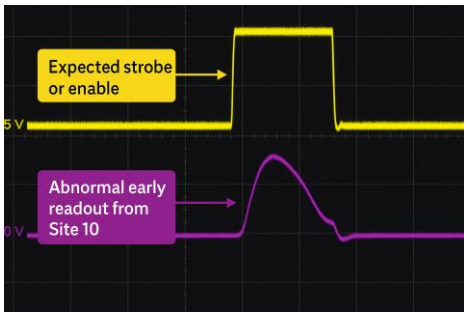

Fig.6. The oscilloscope representation shows two voltage waveforms captured during the first test loop, revealing unexpected signal behavior on Site 10

The waveform shows an abnormal early voltage response on Site 10's readout line (purple) during the first test loop. This response occurs immediately after the strobe signal (yellow) and resembles an analog pulse, rather than a valid digital read. Since no read operation is expected at this stage, the presence of this signal indicates unintentional activity, most likely caused by crosstalk or signal coupling from adjacent sites during full-site testing.

This behavior is isolated to Site 10 and disappears when tested in split-site mode, confirming that the issue is not functional but electrical in nature. The signal shape and timing support the conclusion that Site 10's read path is being disturbed by system-level interference, validating crosstalk as the root cause.

3.3.2 Full-site Activation

Progressive sites enable/disable experiments were performed to isolate the root cause of Site 10's readout anomalies, see Fig.7. The following behaviors were observed:

- Site 10 passes consistently when tested in isolation, confirming that its failure is not due to inherent DUT or test logic issues.
- Site 10 also passes when Site 6 is disabled, indicating a possible coupling or interference path from Site 6 to Site 10.
- When Sites 11 to 16 are disabled, and Sites 1 to 10 remain active, Site 10 passes — suggesting that high activity density from Sites 11–16 contributes to system-level noise affecting Site 10.
- Conversely, when Sites 1 to 8 are disabled and Sites 9 to 16 are enabled, Site 10 still passes, reinforcing the hypothesis that adjacent-site interference, rather than absolute site count, is critical.

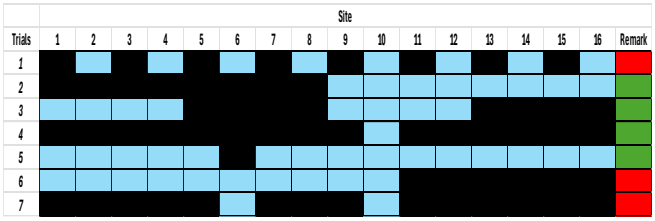

Fig.7. Site enable and disable experiments results; Enabled site (blue), disabled site (black). Remarks : Red (fail), Green (pass)

These results strongly indicate that Site 10's failures are triggered not by functional issues, but by specific inter-site interference patterns under full-site conditions. The pattern of passing results in staggered site activations confirm that electromagnetic coupling or crosstalk from specific neighboring sites, especially Site 6 or regions near Site 10, are responsible for signal integrity violations. These findings further support the effectiveness of split-site or site-group testing as a containment method to suppress these interferences.

Full-site activation increases simultaneous transition and causes crosstalk-related failures on Site 10.

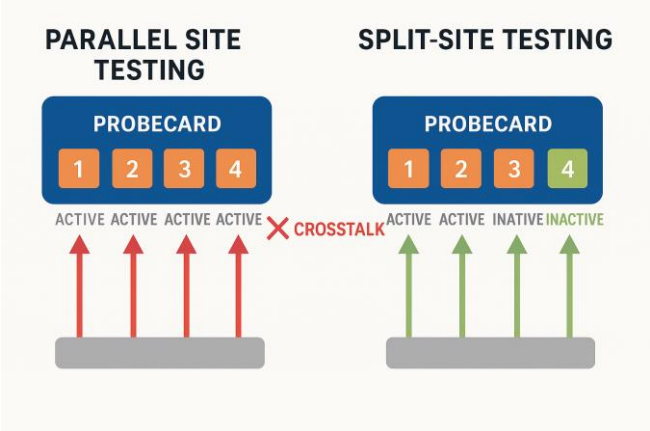

Fig.8. This diagram compares Full-Site Testing (left) and Split-Site Testing (right), visually illustrating how Site 10 is affected by crosstalk during full-site activation and how split-site testing mitigates it.

To isolate the root cause of the Site 10 readout anomaly, split-site testing was deployed, wherein the 16 test sites were divided into smaller activation groups to reduce concurrent switching events. This strategy minimizes simultaneous transitions across the probecard, effectively lowering the system's transient switching noise and inter-site electromagnetic coupling. Under these controlled conditions, Site 10 no longer exhibited consistent premature readback activity, indicating that the read line was previously affected by signal interference during full-site activation.

3.3.3 Micro-cracks and Stack-up Variation

Initial site isolation mitigated crosstalk and improved signal behavior, but not all failures were eliminated. The residual yield loss on Site 10 suggests an underlying structural issue on the probecard. The asymmetry of failures across other sites further supports the hypothesis that PCB-level manufacturing variation is a contributing factor.

Microcracks are typically formed due to mechanical stress and often invisible cracks in copper traces or vias can cause (1) Intermittent connection losses under electrical load, (2) Localized voltage drops affecting signal thresholds, and (3) Site-specific anomalies, especially in repeated probing areas like Site 10.

PCB stack-up inconsistencies, including (1) Variations in dielectric layer thickness, (2) Misalignment of internal copper layers, and (3) Impedance mismatches between layers can all contribute to signal integrity degradation.

These defects are difficult to detect using standard electrical tests and may only manifest under dynamic conditions such as endurance or loop tests. The affected signal path could exhibit intermittent EEPROM communication failures or elevated resistance that pushes the parameter beyond limits.

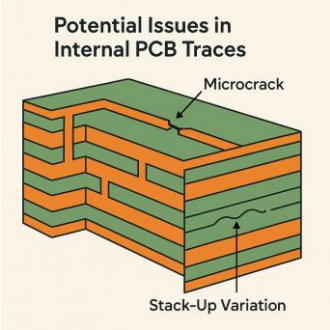

Fig.9. Visual representation of PCB levels on possible micro-cracks and stack-up variation.

Recommended Actions

- *Cross-sectional PCB analysis to validate trace continuity and layer alignment.*
- *X-ray inspection on probecards from failing units to check for via or trace anomalies.*
- *Monitor trace integrity after prolonged thermal/humidity exposure using IST (Interconnect Stress Test) or similar methods.*

Note on Implementation Feasibility:

While the recommended actions such as cross-sectional PCB analysis and X-ray inspection offer valuable insight into potential internal trace defects, these investigative methods are not immediately feasible for urgent resolution due to their specialized nature, required equipment access, and extended turnaround time. As such, these actions are proposed for long-term improvement and root cause validation, rather than as immediate corrective measures within the current production timeline.

3.3.4 Why-why Analysis

To further check on the rootcause, WhyWhy analysis with experts was conducted.

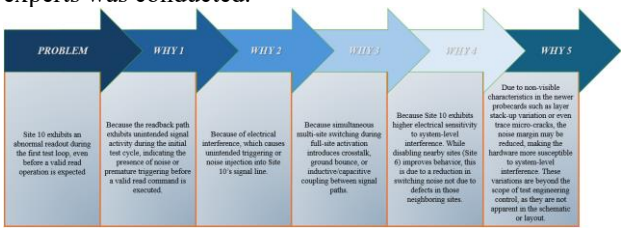

Fig.10. WhyWhy analysis for the abnormal early readouts and multi-site isolation activity

3.3.4 Red X (Root Cause)

Crosstalk-induced signal integrity degradation on Site 10 due to physical and electrical sensitivities of the newer probecards under full-site activation. Abnormal early readout on Site 10 was observed during full-site activation, but not during split-site or isolated testing. Site 10 consistently passed when neighboring sites were disabled, confirming the influence of inter-site interference. This issue is absent on older probecards under identical conditions, pointing to reduced noise immunity in the newer hardware.

3.4 Improve Phase

To mitigate the crosstalk-induced failures observed at Site 10, a Pugh Matrix was assessed for the possible and potential solutions.

Criteria	Weight	Baseline	Buy New Probecards	Split-Site Testing	X-Ray Analysis of Probecard
Cost	5	0	-2	+2	-1
Implementation Time	4	0	-2	+2	-2
Yield Impact	5	0	+2	+1	0
Risk Reduction	4	0	+2	+1	+2
Engineering Resources	3	0	-2	+1	-1
Long-Term Viability	4	0	+2	0	+1
Equipment / Vendor Dependency	2	0	-1	+2	-1
Total Weighted Score		**0**	**+2**	**+24**	**-1**

Fig.11. Pugh matrix for the assessment of solutions

- *Split site testing scores highest due to its low cost, fast implementation, and minimal disruption.*
- *Buying New Probecards has strong long-term benefits but suffers from high cost and long lead time.*
- *X-Ray Analysis helps in diagnostics but adds delays and cost without solving the issue directly.*

Split-site testing emerged as the most practical and immediately impactful solution, offering a balance of low implementation complexity and measurable improvement in yield and signal integrity. This approach requires only software-level reconfiguration within the existing test infrastructure, avoiding hardware changes or capital expenditure. It enables targeted isolation of the affected site(s), effectively mitigating cross-talk without introducing delays to production. The test program was then modified to implement split-site testing, wherein sites are grouped and activated in smaller subsets rather than all 16 simultaneously.

3.4.1 Testprogram revision

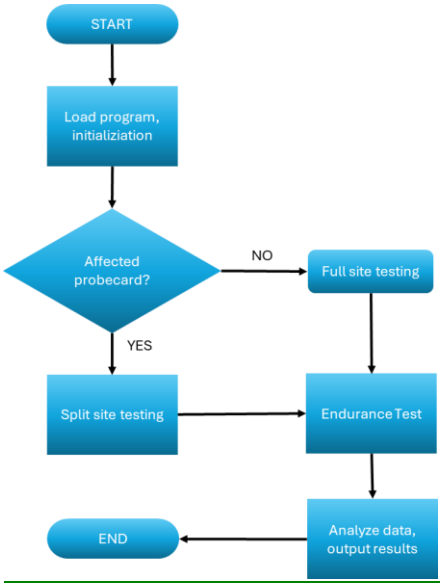

Fig.12. Flowchart for the new test program revision using split site and full site testing depending on the probecard to be utilized

3.4.2 Pilot Run

A pilot run was conducted using the split-site testing configuration on production wafers with the newer probecards. This setup aimed to validate the effectiveness of the mitigation strategy against the previously observed Site 10 readout anomalies. Random failures seen still at site 10 but significantly reduced from 2.15% to 0.91% and accumulated an overall yield of 98.57% comparable to the older probecards that use the full site testing.

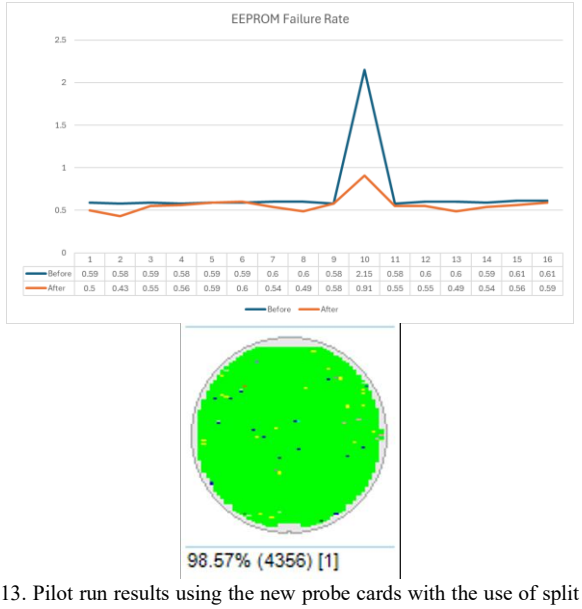

Fig.13. Pilot run results using the new probe cards with the use of split site testing.

3.5 Control Phase

To ensure the effectiveness of the implemented solution while recommended actions for the probecard are being assessed for feasibility and execution, the split-site testing configuration has been formally integrated into the production test flow for units using the new probecards. The updated configuration is locked in the released test program and supported by documented procedures to prevent reversion to full-site activation. Ongoing monitoring of Site 10 yield during pilot and initial production lots confirms the stability of the fix. This control plan ensures that the mitigation remains robust and repeatable, sustaining product quality without requiring hardware changes.

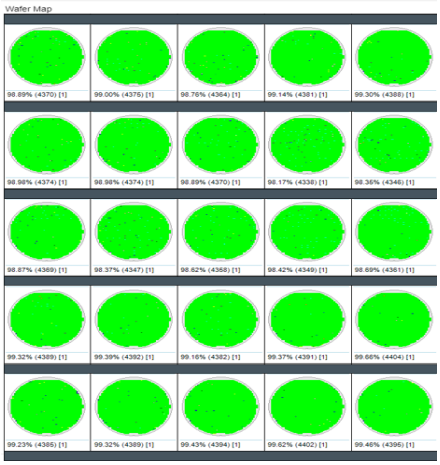

Fig.14. Production wafer maps with yield obtain after split site testing implementation

4.0 RESULTS AND DISCUSSION

Following the implementation of split-site testing as a mitigation for signal integrity issues on Site 10, a pilot run was conducted using the updated test configuration across multiple wafers with the new probecards. The results showed a significant reduction in early readout failures previously observed during full-site activation. Site 10, which had shown inconsistent and abnormal read behavior during the first test loop, passed when tested in split-site mode. Waveform captures further validated the improvement, showing clean readout transitions and no signs of spurious activity.

Site isolation trials played a critical role in confirming that the issue stemmed from inter-site interference, likely caused by increased simultaneous switching noise and crosstalk on the newer probecard design. While the schematic layout remained unchanged, the physical characteristics of the new probecard introduced marginal vulnerabilities under full-site stress. The successful suppression of failure through reduced simultaneous activity supports the hypothesis that the root cause is electrically induced, not functional.

By modifying only, the test software and avoiding hardware replacement, the solution proved to be both cost-effective and scalable. Additionally, it preserved test throughput by optimizing the site grouping strategy. Overall, the observed results support the continued use of the newer probecards under a controlled test environment, with no impact on product coverage or data integrity.

5.0 CONCLUSION

This study addressed a yield-limiting failure observed at Site 10 during full-site testing with newly introduced probecards. Root cause analysis identified the failure because of crosstalk-induced signal integrity degradation, triggered by simultaneous switching of multiple sites. The issue was not observed in older probecards and was reproduced only under high-activity configurations.

Through systematic site isolation, vulnerability was traced to electrical interference rather than functional faults. The implementation of split-site testing effectively resolved the failure without requiring hardware changes, validating the approach as a reliable workaround. The solution was verified in a pilot run, yielding consistent results and restoring expected readout behavior at Site 10.

This outcome demonstrates that test program-level adjustments can be used to compensate for physical design sensitivities, enabling the continued use of new hardware while maintaining test quality and yield.

6.0 RECOMMENDATIONS

It is recommended to continue using split-site testing for all units probed with the new probecards to ensure stable readout performance and avoid crosstalk-related failures. Future probecard validations should also include signal integrity checks under full-site activation to prevent similar issues.

7.0 ACKNOWLEDGMENT

The author would like to thank the Test, Test Product, Test Development Engineering teams for their support during the debug and pilot phases of this study. Special appreciation is extended to the validation team for providing waveform analysis and site isolation data, which were critical in identifying and resolving the root cause. Gratitude is also given to the manufacturing and probecard teams for their collaboration and openness to process-level improvements.

Also, the author would like to acknowledge the mentorship provided by Ms. Annalyn Erni (BB) and Mr. Odelon Garing (BB).

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9.0 ABOUT THE AUTHORS

Aldrin Delos Santos Urriza is currently a Test Engineer at ams-OSRAM. Prior to this, he has experience as Test Product Engineer with 10years of experience working on analysis and improvements both in the field of test and engineering. He has a bachelor's degree in Electronics and Communications Engineering from Laguna State Polytechnic University – Sta.Cruz Main Campus.

Leslie Pearl Lacubtan Carada is the Associate Manager for Test Engineering at ams-Osram. She has 13 years of experience in the semiconductor industry and 3 years in BPO. She earned her bachelor's degree in Electronics Engineering from Mindanao State University – Iligan Institute of Technology.

Joshua Ivan Yray is currently a Test Product Engineer with 2 years of experience at Analog Devices and 5 months in ams-OSRAM. He used his knowledge to provide test solutions and ensure product quality in high-volume manufacturing environment. He has a bachelor's degree on Electronics and Communications Engineering from Technological University of the Philippines - Taguig Campus.