WAFER SAW PROCESS CHARACTERIZATION OF GALLIUM NITRIDE (GaN) WAFER TECHNOLOGY

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[1]New Product Introduction
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ABSTRACT

Gallium Nitride (GaN) wafer technology emerged to support advanced performance and variety of power conversion and radio frequency applications due to its high speed, high temperature, and high-power handling capabilities. This study dwells with the most effective process characterization method to ensure full and consistent device's efficiency were obtained, specifically at wafer sawing process. The test vehicle has Silicon Nitride (SiN) passivation which is known to have low fracture toughness coefficient resulting to passivation peeling or chipping, also it has backside gold metallization compared to standard wafers which require process optimization to acquire the most optimum response. The combination of experimental and analytical methods was used to define the most robust wafer sawing parameters and set-up for this new device. Results showed that after using optimized recipe and application of interval blade dressing function, critical process output responses improved and passed based on requirements. The utilization of wafer saw machine with interval blade dressing function capability was proven to effectively increase the quality and support the most optimum device performance.

1. 0 INTRODUCTION

In manufacturing semiconductor technology, the innovation towards reliable and efficient electronics demands manufacturers wide variety of materials to be considered. The selection of materials has a significant impact on the performance, functionality, and efficiency of the integrated circuit (IC). The most ideal and compatible material should meet the required electrical and thermal properties, have integration capabilities, handle power densities, etc., depending on the application of the electronic device.

Semiconductor industry has been dominated by Silicon throughout the years due to its excellent chemical properties which support stability and reliability of devices. However, in recent years, manufacturers have also been focusing on GaN for specialized applications.

To adapt with fast-paced advancements in semiconductor industry, process characterization specifically at wafer sawing was performed to come up with the most optimized set-up and parameters to support the most optimum device's capability.

1.1 Silicon (Si)

As a dominant material in the semiconductor industry, silicon has proven to be advantageous with its abundance and versatility. Silicon wafer technology as shown in Figure 1 offers excellent electrical conductivity and thermal stability which allows Si to operate at high temperatures, and can be reliably used in microprocessors, memory chips, and integrated circuits.

Figure 1. Silicon Wafer Technology[1]

1.2 Gallium Nitride (GaN)

GaN has a higher breakdown voltage, which allows it to handle higher voltages than silicon to experience an electrical breakdown. This means GaN-based devices can operate at higher power levels without compromising performance. Additionally, GaN wafer technology shown in Figure 2 has higher electron mobility, enabling faster-switching speeds and reduced energy losses compared to silicon. GaN also exhibits operability at higher temperatures, which makes the material ideal for high thermal applications.

Figure 2. Gallium Nitride (GaN) wafer technology[1]

1.3 Gallium Nitride (GaN) vs. Silicon (Si)

As shown in Table 1, GaN devices exceed silicon devices in terms of performance and efficiency, positioning them as a game-changer in the electronics industry. The capability of handling high power has made them suitable for use in electric vehicles, data centers, renewable energy systems, etc.

Table 1. Comparison of Material Properties, GaN vs. Si

Properties	GaN	Si
Thermal Conductivity	100-180 W/m.K	150-200 W/m.K
Electron Mobility	800-2000 cm^2/Vs	1500 cm^2/Vs
Breakdown voltage	600-1200 V/µm	600-900 V/µm
Band gap	3.4 eV	1.1 eV
Power density	High	Low
Switching speed	Fast	Slow

Despite the better performance of GaN, it cannot yet act as a replacement for silicon. Firstly, the abundance of silicon makes it readily available and cost-effective for large-scale manufacturing.

1.3.1 Thermal Conductivity (W/m.K)

GaN devices have excellent thermal and electrical properties with the ability to outperform silicon devices in terms of performance and efficiency.[2] GaN also exhibits operability at higher temperatures, which makes the material ideal for applications including thermal management.[3]

1.3.2 Electron Mobility (cm^2/Vs)

The electron mobility characterizes how quickly an electron can move through a metal.[3] GaN has higher electron mobility, enabling reduced energy losses compared to Si.

1.3.3 Breakdown Voltage (V/µm)

GaN has a higher breakdown voltage than Si, which allows it to handle higher voltages than silicon to experience an electrical breakdown.[3]

1.3.4 Band gap (eV)

Wide band gap of GaN permits devices to operate at much higher temperatures, voltages, and frequencies making the device significantly more powerful and energy efficient than those made from Si.[4]

1.3.5 Power Density

The capability of GaN to handle high power has made them suitable for use in electric vehicles, data centers, renewable energy systems, etc. comparing to Si.[3]

1.3.6 Switching Speed

GaN enables faster-switching speeds, it can switch up to hundred times faster and more efficiently than silicon devices.[3]

1.4 Wafer Sawing Process

The wafer sawing process as shown in Figure 3 separates wafer into individual dice based on die size requirement.[6] The combination of optimized parameters and set-up will result in the most optimum critical process output response.

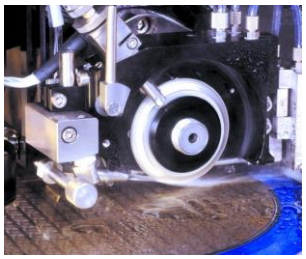


Figure 3. Wafer Saw Process[6]

1.5 Interval Dressing vs. Standard Dressing

Interval dressing is a function to dress a blade during cutting with the dresser board which is mounted on the sub-chuck table shown in Figure 4 (left). This is effective against the deterioration of cutting quality which is caused by continuous processing and decreases the blade clogging and glazing and

leads to the improvement of product quality. Standard dress as shown in Figure 4 (right) uses precut board mounted on tape only. Dressing activity was performed after blade change only prior processing good wafer/s. Differences between interval and standard dress are shown in Appendix A.

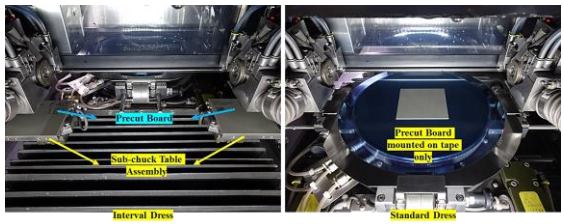


Figure 4. Interval vs. Standard Dress Assembly

2. 0 REVIEW OF RELATED WORK

Refer to 1.0 Introduction.

3.0 METHODOLOGY

3.1 Test Vehicle Description

The test vehicle is stated below on Table 2. The wafer is a 6-inch, non-low-k device with 4 µm Power GaN for RF Gen2 silicon technology. The die size is around 4.000 mm x 0.0900 mm with a die thickness of 70 ± 5 µm and backside gold metallization. Sawing Street is 100 µm.

Table 2. Test Vehicle Information

Test Vehicle	
Wafer size (mm)	150
Silicon technology	Power GaN Gen2 noTSV
Die size (mm)	4.000 x 0.0900
Die Thickness (um)	70 ± 5
Sawing Street (um)	100 x 100

3.2 Process Flow

The process flow is described in Figure 5. The wafer was received mounted, only wafer saw process was performed.

Figure 5. Test Vehicle Process Flow, wafer sawing as focused of the study.

This study will focus on the wafer sawing process. Optimization dwelled only on wafer saw to improve output response. Initial validation shows signature of passivation peeling beyond 5-mm exclusion area of the wafer using defined sawing parameters and set-up by another site. Peeling as shown in Figure 6 was observed but still passed based on defined criteria (not exceeding die external seal ring), requiring fine tuning to improve visual response not affecting other critical process output response.

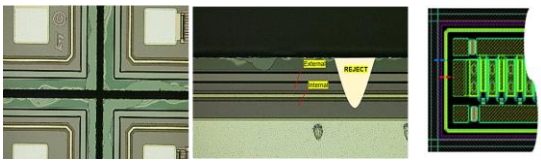


Figure 6. Passivation Peeling observed using POR set-up, and criteria.

Series of evaluation legs as shown in were planned and validated with reference to set-up and recipe defined by another site during fine tuning. Parameters were adjusted based on device requirements.

3.3 Wafer Saw Set-up and Parameters Optimization

Defining critical parameters, set-up, and materials at wafer saw depends on product requirement. Optimization requires a systematic approach to have the most optimum settings for each item without affecting other critical process output responses. Critical parameters used in the optimization are explained in detail as shown in Table 3.

Table 3. Summary of Wafer Saw Parameters Optimized

Parameters	POR	Best Leg	Leg A	Leg B	Leg C	Leg D	Remarks
Z1 Blade	ZH05-SD4000-N1-50 BC						No change
Z2 Blade	ZH05-SD4800-N1-50 AA						No change
Z1 / Z2 Spindle speed	48000 / 20000 rpm						No change
Feed Speed	10 mm/sec				15 mm/sec	10 mm/sec	No change
Z1 cut depth	40 um	49 um	40 um	20 um	40 um	10 um	Deeper Z1 cut
Blade Dress	Standard	Optimized with Interval Dress	Optimized with Interval Dress	Optimized with Interval Dress	Optimized with Interval Dress	Optimized with Interval Dress	Auto dressing included
Blade Dress Frequency	After blade change	After blade change + every 1.5 m	After blade change + every 2.0 m	After blade change + every 2.0 m	After blade change + every 1.5 m	After blade change + every 1.5 m	Interval dress included
Z1 / Z2 Precut Board	F40 / F40	F40 / F50	F40 / F40	F40 / F40	F40 / F50	F40 / F50	Per grit size

3.3.1 Z1/Z2 Blade

Dicing blades are used for grooving, cutting silicon, compound semiconductors, glass, and other materials in the electronic information industry. The selection of the right kind of dicing blade is a prerequisite for good sawing quality.

3.3.1.a Hub Type

The dicing blades combination used for the test vehicle are hub type electroformed blades used for dicing patterned wafers as shown in Figure 7.

Figure 7. Hub and Hub less Blades

3.3.1.b Grit Size

The larger the number, the smaller the grit. Smaller grit particles hit the workpiece material with a smaller amount of force thus resulting in smaller surface chipping.

3.3.1.c Bond Type

In this study, electroformed (hard) bond type dicing blades were used which hold grit strongly thus improving blade life and strength.

3.3.1.d Concentration

The concentration number indicates the percentage of grit in the blade composition. The higher the number, the higher the concentration resulting to improved blade wear out.

3.3.1.e Exposure

Dicing blades used during characterization have shorter blade exposure resulting to small surface and backside chipping.

3.3.1.f Kerf Width

Narrower kerf of dicing blades was used to allow sufficient clearance for chipping and peeling that might be induced during cutting process. Dicing blades combination for this device was considered with the following characteristics shown in Figure 8. When selecting dicing blades to be used, blade life and cut quality is typically the most important criteria but other factors need to be considered like type of material to be cut, production output, dressing blade exposure and wear out, sawing parameters, cutting depth, unit cost, and availability.

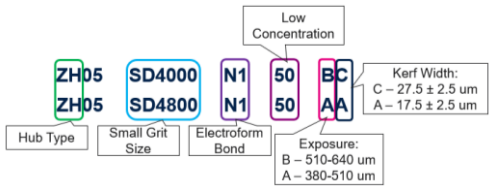


Figure 8. Test Vehicle Blades Specifications

3.3.2 Z1/Z2 Spindle Speed

Higher spindle speed revolutions per minute settings tend to increase blade life and lessen surface chipping thus higher value was set for spindle 1 while lower spindle speed revolutions per minute settings improve blade strength and reduce backside chipping thus lower value was set for spindle 2, thereby facilitating the blade's self-sharpening mechanism.

3.3.3 Feed Speed

As feed speed increases, so does throughput, but because each grain of diamond grit is required to work harder and remove more material per revolution, the stress placed on the blade is greater with high feed speed.

3.3.4 Cut Depth

When cut depth into the tape is shallow, the die retains blade's edge curved shape as shown in Figure 9. Insufficient cut depth tends to cause backside chipping. The greater the process load, results in larger surface chipping.

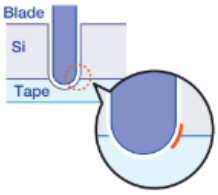


Figure 9. Cut depth is shallow.[7]

Overall wafer saw set-up and parameters depend on factors like workpiece thickness, condition of wafer topside and backside, saw street dimension and condition, and securing force of dicing tape. Optimization then follows to achieve the most desirable output response.

3.4 Process Critical Output Response

Wafer saw process critical output response as shown in Table 4 will be checked if will pass based on criteria after process

parameters optimization and application of interval blade dress function.

Table 4. Wafer Saw Output Response

Process Response	Specification
Topside Chipping and Peeling	Not exceeding die internal seal ring
Sidewall Chippings (Z-axis)	35 µm maximum
Backside Chippings (Y-axis)	35 µm maximum
Die Crack	Any evidence
Kerf Width Z1	25-30 µm
Kerf Width Z2	15-20 µm
Kerf Offset	±3 µm

4.0 RESULTS AND DISCUSSION

Below summarizes the results of the wafer saw parameters optimization performed in the test vehicle and the improvement in the critical process output response specifically topside peeling and sidewall chipping manifestation.

4.1 Wafer Saw Process Critical Output Response

Wafer saw process characterization through parameters optimization, and set-up enhancement by inclusion of interval blade dress function was performed in the test vehicle thus visual inspection, blade cutting conditions, process quality check items, and other critical items are being assessed if within required specifications as follows:

4.1.1 Process Quality Check Items

Using sampling size of ten units (two units per locations including center), topside, sidewall (Z-axis), and backside (Y-axis) chippings were measured and assessed statistically if passed based on requirements and determine most optimum parameters for the device.

4.1.1.1 Topside Chipping

Topside chipping refers to a defect wherein piece of silicon has been removed from die topside. It must not exceed die internal seal ring to be acceptable. Optimization showed significant difference from POR (p value<0.05) as shown in Figure 10.

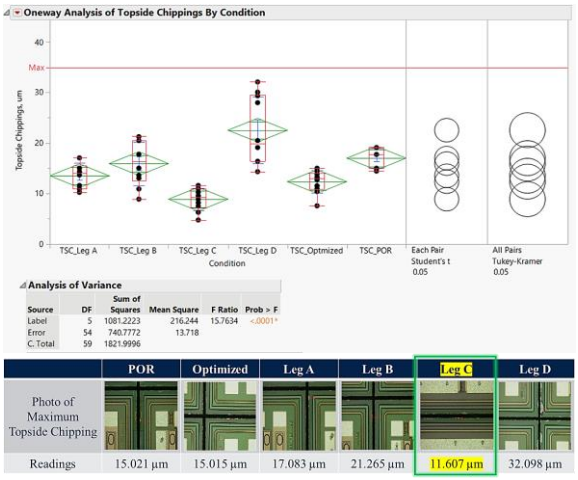


Figure 10. Topside chipping response

4.1.1.2 Topside Peeling

Topside peeling must not exceed die internal seal ring to be acceptable. The topside peeling signature improved as shown in Figure 11.

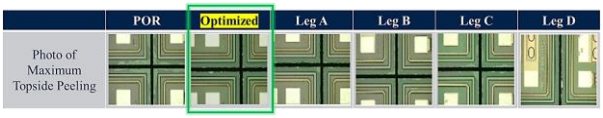


Figure 11. Topside peeling response

4.1.1.3 Sidewall (Z-axis) Chipping

Sidewall chipping must be half of wafer nominal thickness. Optimization showed significant difference from POR (p value<0.05) as shown in Figure 12.

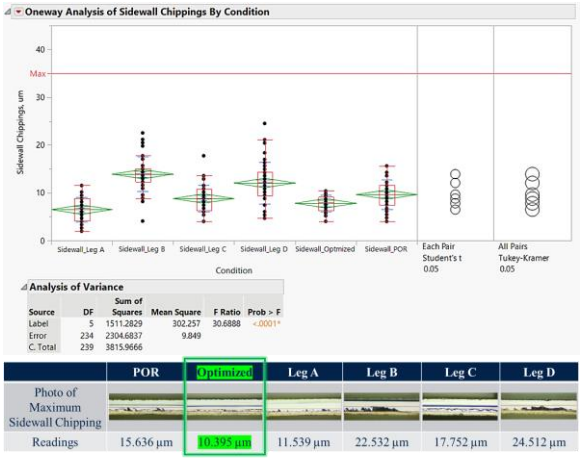


Figure 12. Sidewall chipping response

4.1.1.4 Backside (Y-axis) Chipping

Backside Chipping refers to a defect wherein piece of silicon was removed and manifested at die backside. It must be half of wafer nominal thickness. Optimization showed comparable result POR (p value>0.05) as shown in Figure 13.

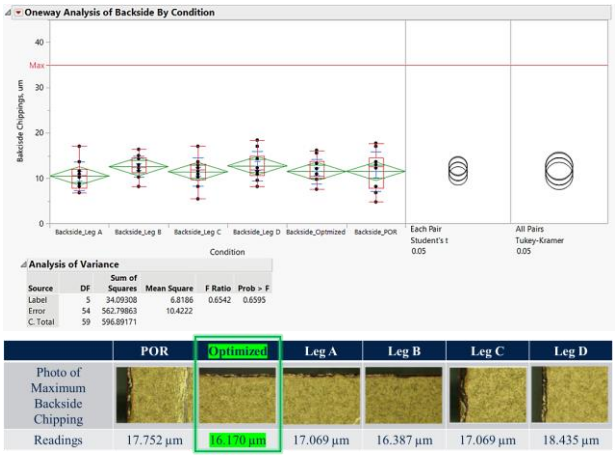


Figure 13. Backside chipping response

4.2 Process Time

Process Time is the amount of time it takes to complete the cutting process of one wafer. [6] Approximate 27.62% decreases in processing time per wafer including blade dressing as shown in Figure 14.

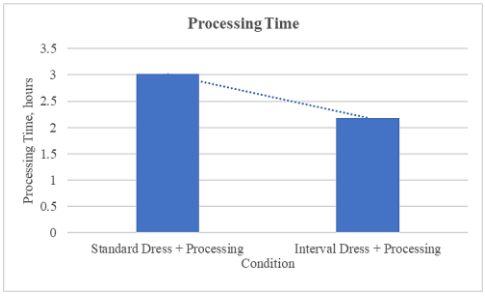


Figure 14. Processing Time, standard vs. interval dress.

4.3 Blade Wear out

Blade wear out refers to gradual decrease in blade's exposure upon usage. Average blade wear out for POR and optimized for both spindles are within criteria as shown in Figure 15.

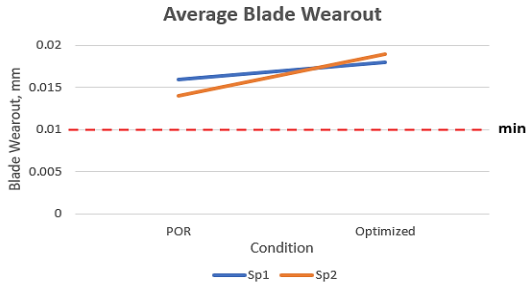
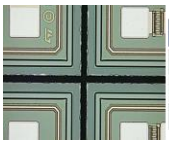


Figure 15. Average Blade Wear out

4.4 Kerf Width and Kerf Offset

Kerf Width refers to the material's size removed during dicing process and passed for both spindles based on criteria.

Kerf Offset refers to centering of blade kerf with respect to \ sawing street and passed based on criteria of ± 3 µms.[6] Kerf width and offset data are shown in Figure 16.



Item	Criteria	Min	Max	Average
Kerf Width – Z1 (µm)	27.5 ± 2.5	25.729	29.635	28.588
Kerf Width – Z2 (µm)	17.5 ± 2.5	16.497	18.816	18.111
Kerf Offset (µm)	±3	0	1.60	0.69

Figure 16. Kerf Width and Kerf Offset Data

4.5 Visual Inspection

As additional checking, post process visual inspection results shown in Figure 17 show no major issue after process parameters optimization. Kerf width is centered and within specifications based on blade type requirement. No out of specification chipping, crack, and peeling observed.

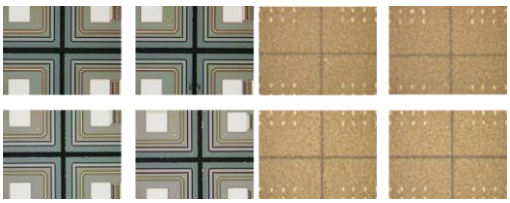


Figure 17. Post Saw Topside and Backside Visual Inspection Results

4.7 Summary of Process Output Response

Based on the assessment of the optimization results, shown in Table 5, critical output response at wafer sawing passed all the defined requirements of the test vehicle.

Table 5. Summary of Wafer Saw Output Response

Process Response	Specification	Results
Topside Chipping and Peeling	Not exceeding die internal seal ring	Passed
Sidewall Chippings	35 µm maximum	10.395 µm
Backside Chippings	35 µm maximum	16.17 µm
Die Crack	Any evidence	Passed
Kerf Width Z1	25-30 µm	29.635 µm
Kerf Width Z2	15-20 µm	18.816 µm
Kerf Offset	±3 µm	1.60 µm

Optimized parameters or the best leg was defined based on quality of cutting response in the wafer. Data shows that optimized parameters showed the most optimum response in terms of topside peeling, sidewall, and backside chipping response.

5.0 CONCLUSION

In this study, it has been shown that defined optimized parameters and addition of interval blade dress function improved critical process output response and overall device's performance. Topside peeling and sidewall chipping manifestation was effectively improved using optimized blade dress recipe, and interval blade dress function which supports blade sharpening during wafer processing and enhanced cutting response.

6.0 RECOMMENDATIONS

The authors recommend to include interval blade dress function capability to wafer sawing machines to enhance process output response. For new devices with same wafer technology as the test vehicle, use the defined optimized parameters as reference and perform further optimization based on wafer's topside condition, wafer thickness, saw street dimension, and condition, and device requirements. For future studies, check feasibility of using higher feed speed settings and further optimization of other process parameters to reduce processing time without compromising critical process output response.

7.0 ACKNOWLEDGMENT

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10.0 APPENDIX

Appendix A – Standard vs. Interval Dress Parameters

Type of Dress	Dress Frequency	Spindle	Precut Board	Step 1			Step 2		
				Depth (µm)	Speed (mm/s)	Lines	Depth (µm)	Speed (mm/s)	Lines
Standard	Every blade change	Z1	F30	200	10	1	200	40	14
		Z2	F30	200	10	1	200	40	14
Interval	Every blade change	Z1	F30	200	10	1	200	40	28
		Z2	F50	250	10	10	100	50	15
	Every 1.5 m	Z1	F30	300	20	5			
		Z2	F50	200	20	5			