THREE-WAY TEST DETECTION ENHANCEMENT: A BREAKTHROUGH SOLUTION FOR SOLDER CRACK MARGINAL OPENS

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ABSTRACT

The introduction of HotRod™ Quad Flat No Lead (QFN) packaging technology gave way to a smaller and more efficient semiconductor packaging solution for Power Products. However, this also introduced new challenges to Quality. Making use of solder bumps instead of the traditional wirebond introduced a new interconnect defect to QFN assembly process – Solder Crack.

With the ramp-up of HotRod packages, there was also an increase in Solder Crack related customer returns. Solder Crack defects reaching the customer means the traditional Final Test detection and screening, Continuity Test, is insufficient. This paper aims to address gaps in Final Test detection, ensuring timely feedback to Assembly process and improving overall customer satisfaction.

Solder crack modeling thru characterization of customer returns show that marginal resistive open failures pass the current Continuity Test coverage. This three-way test detection enhancement is a breakthrough solution for detecting Solder Crack marginal open failures thru Limit Characterization, Marginal Opens Test and Continuity Delta Test.

1. 0 INTRODUCTION

A Flip Chip on Lead (FCOL) package makes use of solder bumps as an interconnect between the silicon chip to the package instead of the traditional wire bonding. HotRod™ is a FCOL type QFN package technology incorporating the lower resistance of traditional FCOL with improved electrical and thermal performance of a QFN over traditional leaded packages.

HotRod™ QFN has become an important packaging option for power devices in TI as it offers a more efficient and smaller packaging solution – both needed to catch-up with the ever miniaturization trend in semiconductor solutions.

1.1 HotRod™ QFN vs Wirebond QFN Packaging

Wirebond QFN package is typically restricted to approximately 0.4 Die Area to Package Area (DAPA) due to design rules and assembly manufacturing limitations e.g. wire loop profile. HotRod™ QFN can support up to 0.75 DAPA ratios thus offering higher power densities and smaller package footprint for the same silicon chip size.

Characteristic	Wirebond QFN	HotRod™ QFN
Package Size		√
Parasitics from Pin to Die		√
Power Loss		√
Thermal Pad Thermal Performance	√	
Cost	√	
Complexity	√	

Legend:
√ = Better

Fig. 1. Comparison of HotRod QFN to Wirebond QFN.

1.2 HotRod™ QFN Assembly

HotRod™ QFN utilizes a bumped die which, depending on current requirement and optimized package size, can either be circular or oval. The leadframe design utilizes selective plating in line with the bumped die for die attach. The bumped die is then flipped over and attached to the leadframe via solder reflow to form the interconnect between die and package.[1]

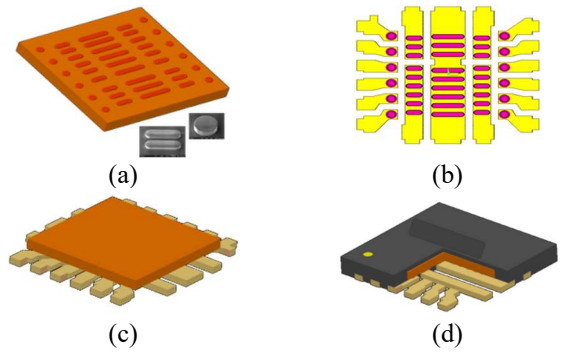

Fig. 2. (a) Bumped die showing the oval and circular bump shapes, (b) Leadframe with selective plating for bonding, (c) Silicon chip attached to the leadframe and (d) Overview of the molded package.

1.2.1 HotRod™ Package Interconnect Structure

The silicon chip Cu post bump is connected to the leadframe via solder reflow to for the package interconnect.

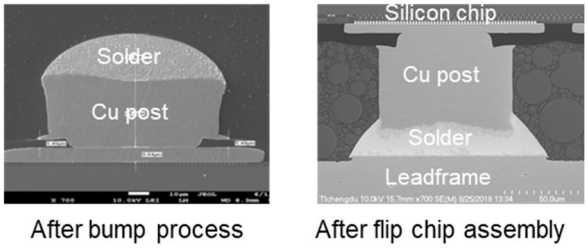

Fig. 3. Bump structure after bump process and Silicon chip interconnect after flip chip Assembly process.

1.2.2 HotRod™ Package Interconnect Defects

The introduction of this new packaging technology brought about new challenges in the Assembly process. This includes new interconnect defects which are Solder Crack and Non-wets. As shown in Fig. 4, Solder Crack is a separation due to a crack within the solder joint while Non-wets is when the Silicon bump is not wetting or soldering with the leadframe. Both defects can be caused by material, process or design issues.

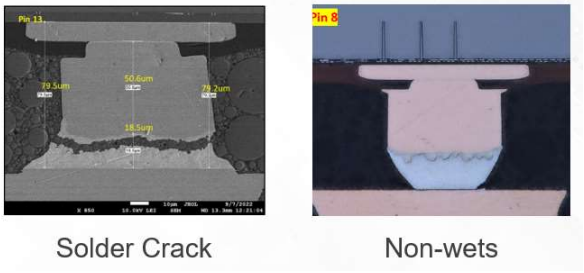

Fig. 4. HotRod™ interconnect defects.

1.3 HotRod™ Solder Crack Customer Return Cases

As more Devices prefer the HotRod™ packaging option and continue to ramp-up, TI Clark has noted an increase in customer returns due to Solder Crack affecting Customer Satisfaction. These defects reaching the customer means that current detection and screening controls in the Assembly and Test (A/T) site is insufficient.

Fig. 5. shows high annual Solder Crack cases during HotRod™ QFN ramp-up in 2018

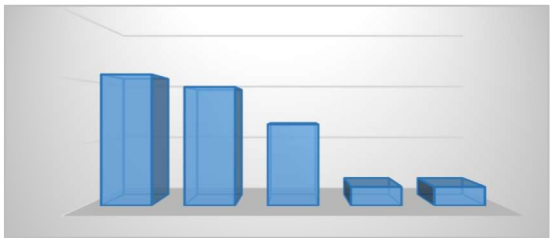

Fig. 5. Solder Crack Customer return cases

1.4 Solder Crack Final Test Coverage

The conventional way in detecting and screening out interconnect integrity defects in a semiconductor Integrated Circuit (IC) chip is thru Final Test Continuity Test. This ensures the silicon chip has proper connection with the leadframe after assembly packaging. Continuity Test checks the continuity between the Automated Test Equipment (ATE), IC package and Silicon Chip. This is usually done by forcing a small current on to the IC pins and measuring the corresponding voltage to determine whether a shorts or opens is present indicating a defect.

A separation in a HotRod™ QFN's interconnect, whether Solder Crack or Non-wets, corresponds to an open connection between the silicon chip and leadframe. This in turn is expected to be detected during Final Test Continuity Testing as an open failure defect. A good Final Test coverage should be able to screen out Solder Crack or Non-wet defects regardless of interconnect resistance – whether hard opens or marginal.[2]

1.4 Solder Crack Marginal Opens

Marginal opens are defects with small resistance between silicon chip to leadframe due to interconnect separation – still close enough to conduct electrical current at time zero Final Testing but poses reliability risks and may fail at the Customer.

The challenge in zeroing out Solder Crack related customer returns is in detecting and screening marginal opens during Final Test.

2. 0 REVIEW OF RELATED WORK

Refer to 1.0 Introduction.

3.0 METHODOLOGY

3.1. Electrical Characterization

To address Test detection of solder crack and non-wets marginal opens, three methods are used which includes review of customer return units test result and existing test solution, solder crack and non-wets modeling and simulation, and three-way test detection enhancement and validation.

3.1.1. Review of Customer Return Unit Test Result and Existing Test Solution

To begin with, the history of customer return units with solder crack and non-wets defects are reviewed which includes customer problem description, the type of issue seen, suspected pins, and retest result of the units. The failing tests are considered and their test methods are analyzed.

Continuity Testing verifies interconnect integrity by detecting the presence of electrostatic discharge (ESD) protection diodes. During this test, all device pins are subjected to zero volts, current is forced and ESD diode voltage is measured. In case of an open connection, and open circuit compliance voltage is measured.

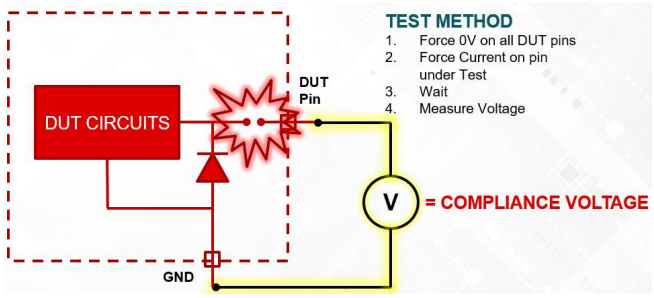

Fig.6. Continuity testing with compliance voltage is measured.

In analyzing the continuity test method, the test program routine is reviewed which includes correctness of tester resource to device pin connections, currents and/or voltages to which the device pin is subjected, and measurements taken from the device pin. In addition, the lower and upper limits are reviewed.

3.1.2 Solder Crack Modeling and Simulation

Solder crack and non-wets marginal opens in the device pin interconnects are equivalent to a small resistance in series connection to the ESD diode between the die pin and the device under test (DUT) pin. With this type of connection, the resulting voltage measured during continuity test will come from both the ESD diode and the solder crack voltage.

3.1.3. I/V Curve Analysis

Sample good units, full opens and marginal opens solder crack and non-wets defects are tested then subjected to current/voltage (IV) curve analysis to analyze the ESD diode forward bias region voltage response where the voltage values of the full opens and marginal opens fails are compared to that of the good units.

3.2 Test Escape Fault Tree Analysis (FTA)

To further deep-dive into solder crack and non-wets marginal opens, FTA tool is used. Here all of the possible root cause of non-detection at Test are identified and analyzed.

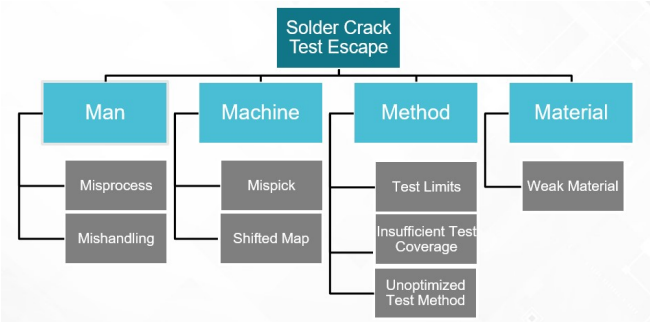

Fig.7. Solder crack test escape Fault Tree Analysis

3.3. Three-Way Test Detection Enhancement and Validation

There are three ways to enhance Test detection of solder crack derived from the electrical characterization and test escape FTA which include test limit tightening, marginal opens testing and delta continuity testing. Test limit tightening refers to adjusting the test limit to a voltage value able to screen out added resistance. Marginal opens testing is a two-point continuity test using two different higher forcing currents and measuring corresponding voltages to compute solder crack resistance using the established equation. Delta continuity testing involves continuity testing before and after parametric and functional tests. Stress test is also incorporated before final continuity testing to force fail marginal failing units.

To measure enhanced Test detectability, all three methods are applied to sample good units, full and marginal opens fails then validated.

4.0 RESULTS AND DISCUSSION

4.1. Electrical Characterization

Electrical characterization started off with the review of historical test data from solder crack and non-wets defects. Reject units that passed time-zero testing were separated into hard opens fails from full opens fails and marginal opens failures. The number of marginal opens fails are slightly lower than that of hard open fails.

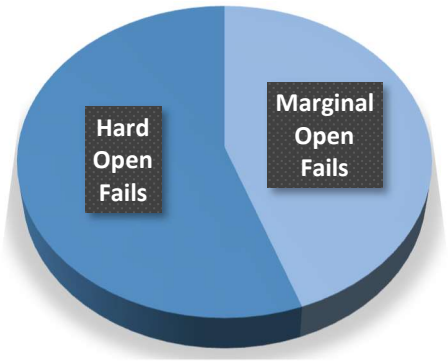

Fig.8. Solder crack and non-wets categorized into hard and marginal fails.

The existing test solution that screens out solder crack was reviewed. During continuity test, units are subjected to zero volts on all device pins, current is forced and ESD diode voltage is measured. In case of an open connection, the compliance voltage of an open circuit is measured. The test method proves that opens fails are detectable.

Modeling solder crack into the circuit, a small resistance is seen between die pin and the DUT pin which when now measured results to an added voltage in addition to expected ESD diode voltage.

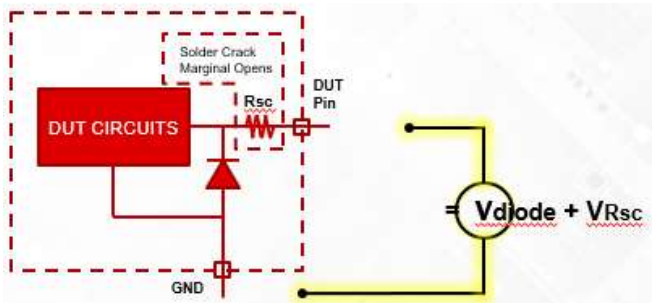

Fig.9. Continuity testing with solder crack resistance Rsc.

Sample good units, rejects and marginal opens were tested and subjected to IV curve analysis to analyze ESD diode forward bias voltage response. With a 0.3mA forcing current, normal diode response is observed for a good unit, higher voltage for a marginal open reading, and the highest voltage for a reject unit. Counterchecking with continuity test limits, reject unit failed while the marginal opens and good unit passed. Apparently, marginal opens can be screened out by tightening the test limits.

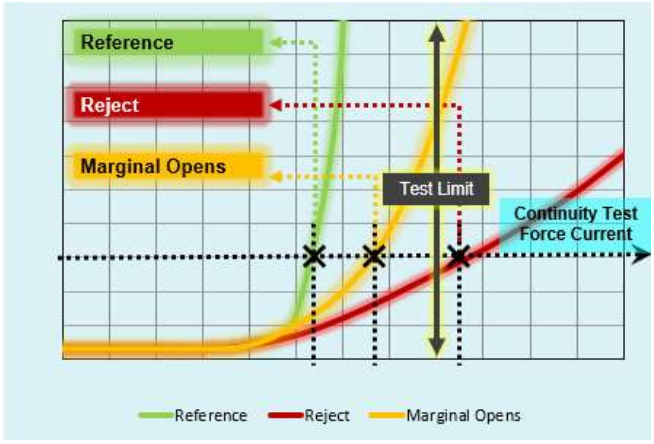

Fig.10. Current vs. Voltage (IV) Curve Analysis

On the other hand, with higher currents, resulting voltage difference with respect to good unit is now more apparently farther from the good unit voltage. Using two points on a marginal unit, solder crack resistance can now be measured by deriving from Ohm's law where the solder crack resistance is equal to the change in voltage over the change in current.

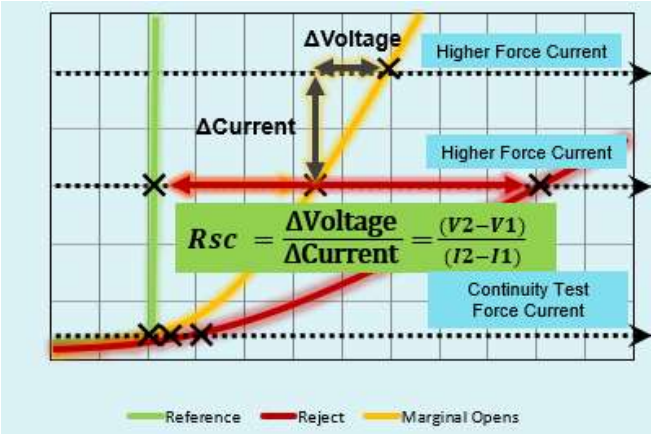

Fig.11. Deriving solder crack resistance from (IV) Curve Analysis

4.2 Test Escape Fault Tree Analysis (FTA)

From solder crack test escape FTA, two causes are determined: test limits and insufficient test coverage.

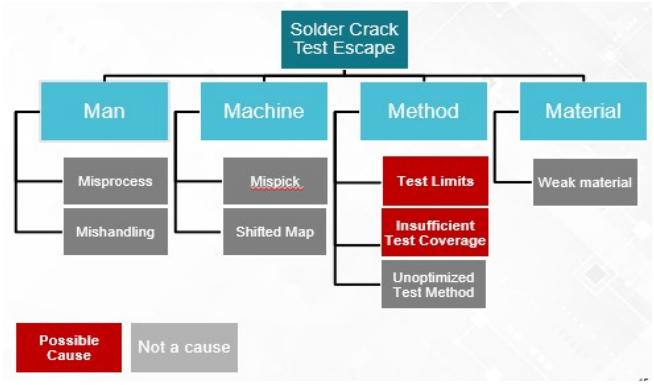

Fig.12. Test Escape FTA

Using such findings, conventional or existing continuity test can now be innovated with the three-way test detection enhancement including continuity limit tightening, marginal opens testing and continuity delta testing.

4.3. Three-Way Test Detection Enhancement and Validation

4.3.1. Continuity Test Limit Tightening

From I/V curve analysis, accurate tighter limits have been determined to screen out potential solder crack defects while maintaining an acceptable Cpk. Through outlier detection, it has been confirmed that marginal solder crack defects with a certain resistance value are detectable.

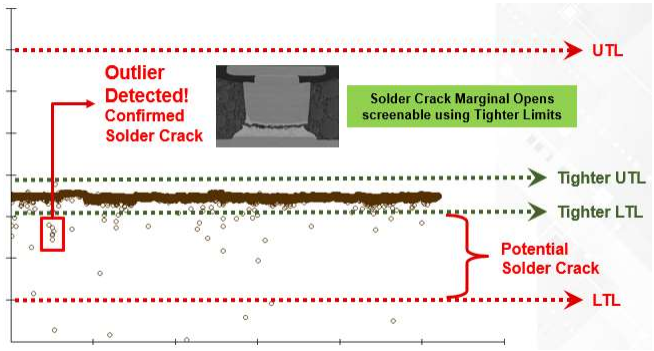

Fig.13. Solder crack marginal opens detected through tightened test limits

4.3.2. Marginal Opens Test

A new method is introduced to measure solder crack resistance. This is a two-point continuity test using two different higher forcing currents (vs. conventional) and measuring corresponding voltages to compute solder crack resistance using the established equation. With a Kelvin connection, it can screen out solder crack marginal opens up to a certain lower resistance value.

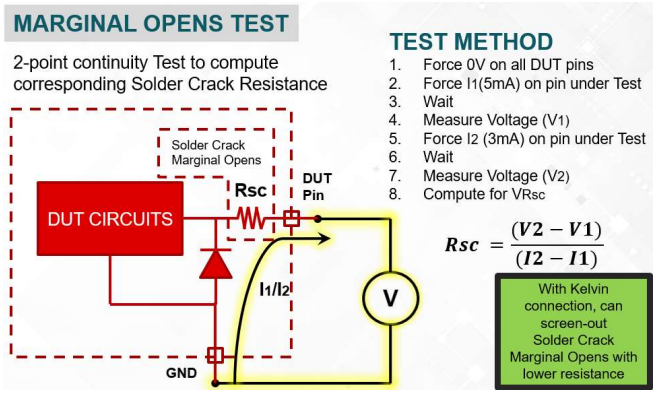

Fig.14. Marginal Opens Test

4.3.3. Continuity Delta Testing

The final innovation to detect solder crack and non-wet marginal opens fails is to incorporate stress test during time-zero testing. Solder crack with a very small resistance value acts like a fusible resistor that when stressed using absolute maximum voltage rating will break, causing hard opens similar to what is seen on customer returns. With the incorporation of stress test followed by continuity delta testing, the remaining marginal opens with the lowest resistances can now be zeroed out.

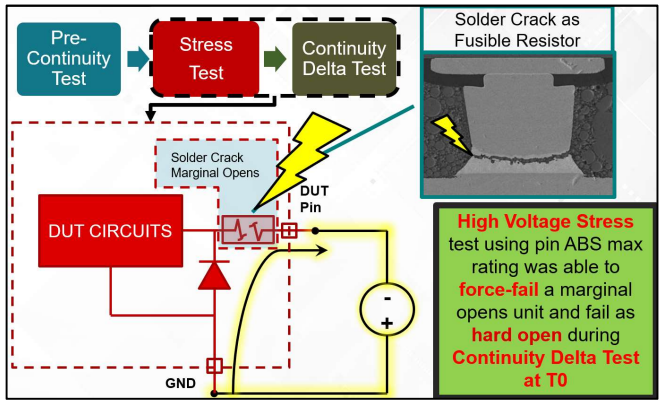

Fig.15. Continuity delta test after application of high voltage stress.

5.0 CONCLUSION

Solder crack and non-wets elimination by the three-way test detection enhancement proved to be successful. Review of defect testing result and existing test solution, solder crack modeling and simulation enabled defect characterization and allowed for the implementation of effective test limits for solder crack and non-wets detection. I/V curve analysis proves that there are voltage response differences among good, full open and marginal opens and that they can be used to derive a new testing method for detection. Incorporating stress test during time zero testing and performing delta

continuity testing after stress proved to be effective in detecting marginal opens.

This enabled elimination of customer return impact contributed by solder crack and non-wet marginal open defect types and lowered total overall customer satisfaction year-on-year. This also resulted to $45k cost savings.

6.0 RECOMMENDATIONS

It is recommended to fanout implementation of three-way test detection enhancement across all HotRod™ devices. A further study of stress testing as a means to force-fail reliability failures is also recommended.

7.0 ACKNOWLEDGMENT

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9.0 ABOUT THE AUTHORS

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