USING "SETUP PARAMETRIC" TO IDENTIFY AND RESOLVE "BAD SITES" ON MULTISITE SETUP

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ABSTRACT

In the semiconductor industry, the growing demands for higher parallelism have led to the introduction of new testers and handlers. However, maintaining a multisite operation with all sites enabled and yielding has remained a persistent challenge, with only a few sites running on average due to setup problems. As the number of sites increases, so does the likelihood of encountering issues.

Traditionally, troubleshooting methods have involved replacing multiple hardware parts and running quick tester diagnostics. These methods often lead to more downtime and, worse, fail to identify the root cause of the problem.

This paper introduces the concept of setup parametric analysis as an alternative method for determining setup issues. It also presents a structured approach to parameter selection and optimization in the context of a multi-site semiconductor device testing setup. This approach aims to identify and resolve issues that may adversely impact the system's performance and reliability. The paper demonstrates that by checking these setup parameters before applying traditional troubleshooting methods, it is possible to achieve quicker identification and resolution of setup problems, ultimately improving overall multisite yield and efficiency.

Based on the pilot study involving over 2 million devices tested, the 'setup parametric analysis' significantly increased the yield from 25% to 90%.

1. 0 INTRODUCTION

In the rapidly evolving semiconductor industry, the demand for higher parallelism has driven the adoption of multisite handler testing, with 16/32 sites becoming the norm (ITRS, 2015). This advancement in testing capabilities has the potential to significantly improve production efficiency and throughput. However, maintaining all sites enabled and yielding has remained a persistent challenge in the industry.

Typically, with a problematic setup, only 50%-70% of the available sites are running on average, with the remainder being disabled due to low yield, also known as "bad sites" (Kang et al., 2019). The root causes of these issues are varied and complex, often requiring extensive troubleshooting efforts.

The traditional method of troubleshooting such problems often involves replacing the load board, mechanical hardware, or running tester diagnostics to identify defective tester boards (Mogensen, 1997). This approach, while commonly used, may not always effectively identify the root cause of the problem, leading to prolonged downtime and suboptimal productivity. To address these challenges, a more systematic and comprehensive approach to troubleshooting is necessary. As the principle states, "we cannot solve problems that we cannot see; seeing is everything" (Deming, 1982). By gaining a deeper understanding of the underlying factors that contribute to the poor multisite performance, manufacturers can develop more effective strategies to identify and resolve the root causes, ultimately improving overall yield and efficiency.

1.1 Introducing the concept of Setup Parametric

While exploring alternative methods to determine bad sites, we developed the concept of setup parametric. We studied how they relate to site yield and realized they could indicate if a site is bad. Apparently, analysis shows that a big number of bad sites are due to poor setup parametric and not due to the hardware. See Figure 1.

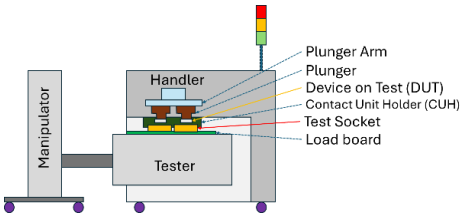

Fig. 1. Typical hardware for Tester/Handler setup. The device testing hardware comprises a plunger arm that pushes devices into the test socket, which connects to the tester load board and is evaluated for electrical performance.

1.2 The 3 Setup Parameters

Setup parametric involves basic handler mechanical and thermal condition checking. We have identified three Setup parameters that will serve as our metrics for checking the condition of the setup and identifying bad sites, the Plunger force (1), test site temperature (2), and front arm vs. rear arm reject clustering (3). These three have been identified as significant parameters and are proven to be good indicators of handler performance. Checking them before applying the traditional method can result in quicker identification and fixing of bad sites.

2. 0 REVIEW OF RELATED WORK

In the highly complex and interconnected world of semiconductor device testing, ensuring consistent performance and reliability across multiple testing sites is a critical challenge. Identifying and addressing parameter misalignment or suboptimal configurations that lead to problematic "bad sites" is essential for maintaining the integrity of test results and optimizing the overall testing process.

2.1 Engineering design selection using parametric approach.

Similarly, the paper "Optimal Parameter Selection in Engineering Design" by Kyoung-Yun Kim and Wei Chen explores the critical role of parameter selection in engineering design processes. The authors present a framework for identifying the optimal set of parameters that best capture the problem at hand and lead to effective solutions.

The paper emphasizes that the selection of appropriate parameters is a crucial step in the engineering design process, as it directly influences the accuracy and effectiveness of the final solution. The authors argue that a systematic approach to parameter selection can help designers navigate the complex trade-offs and interdependencies among various design factors.

The proposed framework outlines a methodological approach to parameter selection, which involves identifying the relevant parameters, understanding their relationships and interactions, and optimizing the parameter set to achieve the desired design objectives. The authors demonstrate the application of their framework through case studies, illustrating its practical utility in real-world engineering design problems.

Overall, the paper provides valuable insights into the importance of parameter selection in engineering design and offers a structured approach to address this critical aspect of the design process.

3.0 METHODOLOGY

3.1 Plunger Force as 1st setup parameter

The latest Multisite handlers employ a regulated plunger force per site. The desired force can be inputted through the handler O/I. Normally the force should match the socket pin spring force to ensure the best contact condition between the DUT and the socket pins. Too low force is not good for the yield. Too high a force is indicative of a defective plunger part. In both cases, the plunger will need to be checked and repaired.

An in-house tool was designed to measure the force exerted by each of the 16 plungers individually, enabling the identification of specific plungers requiring inspection. This tool utilizes dedicated load sensors, one for each plunger site, which are sequentially connected to a reader to accurately measure the force exerted by the plungers at different test sites. See Figures 2 and 3.

Fig. 2. Plunger Force Profiler. This is an actual picture of a force reader connected to the 16sites CUH with sensors embedded per site.

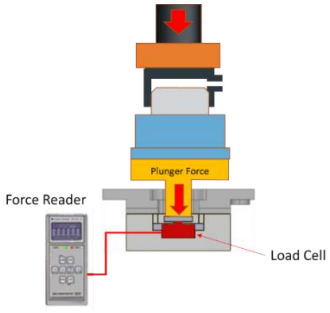

Fig. 3. Plunger Force Profiling Tool Schematic. The figure shows a DUT that is being plunged to the sensor/Load cell that generates small electrical signal and translated to a Force (N) by a handheld reader.

3.2 Test Site Temperature as 2nd setup parameter

The latest Multisite handlers now come equipped with Active Thermal Control (ATC) technology, allowing each test site to have independent thermal control capabilities to precisely meet the temperature requirements of the Device Under Test (DUT). Failure to optimize the temperature settings for a specific test site can result in decreased yield, particularly if the DUT contains temperature-sensitive parameters. Any deviations in the test site temperature, whether exceeding the desired range by being too high or too low, can lead to a shift in the distribution of these temperature-sensitive parameters beyond acceptable test limits.

Determining the appropriate test site temperature involves more than just using a simple ***"device sensor"*** to measure temperature. This conventional method provides a controlled condition but fails to consider the intricate "thermal dynamics" that can occur between the socket, device package, and test program.

In real production conditions, these thermal dynamics become evident as heat may transfer into or out of the DUT during the testing process. The ability to monitor and analyze these dynamic thermal transfers is crucial for identifying problematic test sites. Tracking a ***"temperature-correlated"*** device parameter through multiple plunging cycles during production testing can offer valuable insights into site performance. For instance, in the case of an Advanced Driver Assistance Systems (ADAS) device, the plot of Reg_Vdiode, a temperature-correlated device parameter, can help reveal signatures of problematic sites, such as site 0 and site 2 in the example provided. See Figure 4.

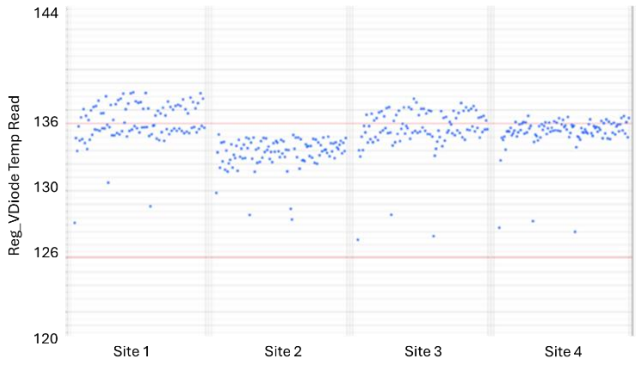

Fig. 4. Bad Reg_Vdiode Temp Read. The graph shows the tracking of Diode temperature reading every insertion per site.

3.3 Front Arm vs Rear Arm Reject Clustering as 3rd setup parameter.

Typically, Multisite handlers employ two arms (Front and Rear) that alternately plunge into the test sites, 16 DUTs at a time. This is used to eliminate down time during changeover of devices from batch of devices to the next. Each arm is like an ecosystem on its own and can behave differently from the other. See Figure 5.

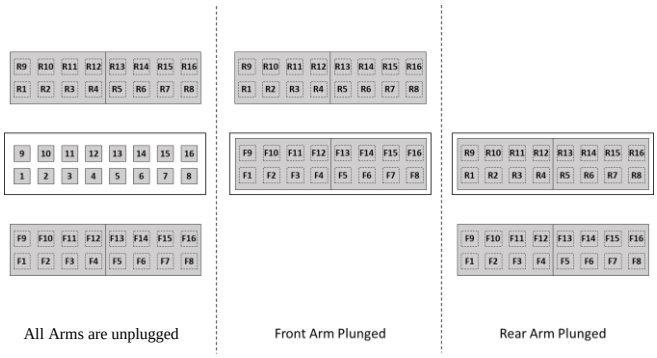

Fig. 5. Plunger batching. The middle diagram shows the Front Arm plunged into the test site. The right diagram shows the Rear Arm plunged into the test site.

One arm could yield OK, while the other would be causing bad sites. The key is to separate the test results between the Front and the rear arms for easy detection of bad sites due to a bad arm and looking for "clustered rejects." See Figure 6.

Note that there is a clustering of rejects on Site 0 on the Front Arm, while the Rear Arm yield is OK. The Front Arm will need to be checked for mechanical alignment, especially on site 0.

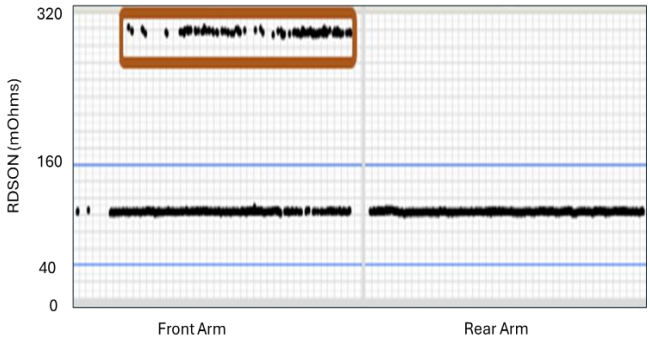

Fig. 6. Separated RDSON Measurements. The figure shows the separation of Front Arm data and Rear Arm data to reveal "clustered rejects."

4.0 RESULTS AND DISCUSSION

4.1 Plunger Force Measurements

Using the plunger force tool, we have been able to visualize the distribution of force per plunger on 16 sites. Note that sites 3 & 11 have very low readings resulting to a very low production yield around 44%. Based on the force parameters (Figure 7), there are sites with force measurements lower than the expected 11.5N setpoint. Upon checking the hardware, air leakages were noticed coming from the barb fitting of Site 3 (Figure 8) and from a tear in the diaphragm of site 11 (Figure 9).

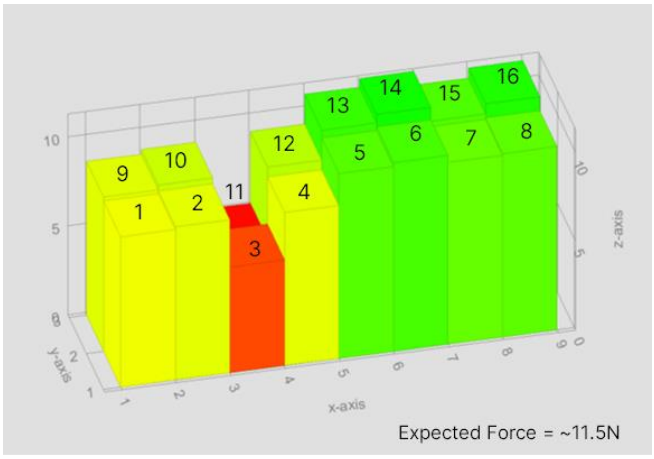

Fig. 7. Plunger Force distribution graph. This data was taken from one of the problematic handler setups.

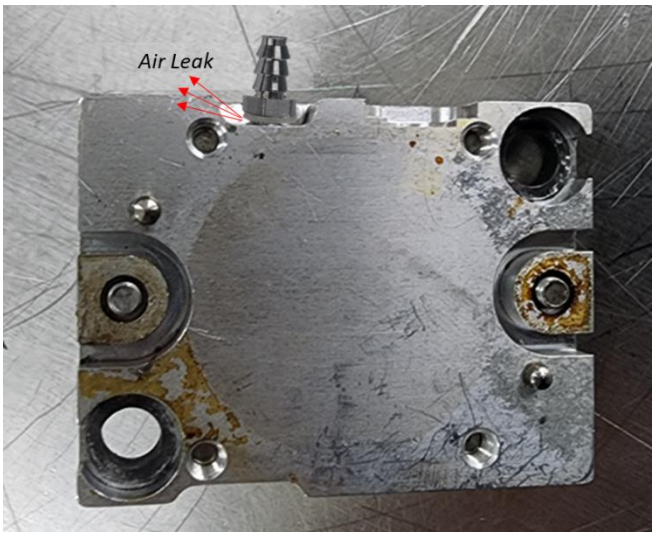

Fig. 8. A picture of actual plunger parts with problem. See that the barb fitting was not installed properly and causing air to leak out.

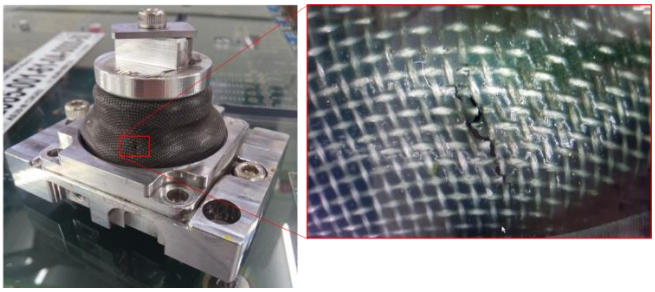

Fig. 9. A picture of an actual plunger diaphragm. This is a part of the plunger that controls the Plunger force by air pressure. There is a tear diaphragm causing air leak.

After fixing the mechanical parts of the handler, we performed the same procedure again to verify the actual force on 16 sites. It appears that all the expected forces are now normalized (Figure 10) and within the expected 11.5N setpoint. We also cycled several devices for testing and the result looks good yielding 100% at all sites (Figure 11).

Fig. 10. Plunger Force distribution graph after the fix. Plunging Force on all sites normalized after fixing the leaks.

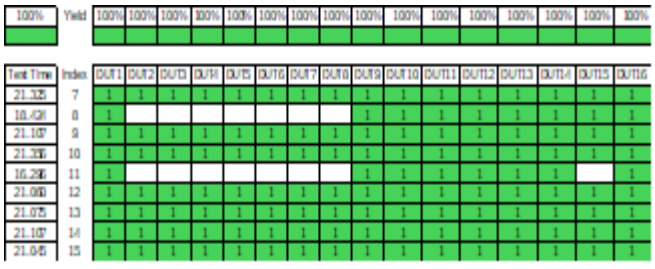

Fig. 11. Test results table. The figure shows good test results after fixing the mechanical parts of the Plunger.

4.2 Test Site Temperature Measurement

The previous figure shows a temperature-correlated parameter Reg_Vdiode (Figure 4), which, in this case, is tracked through several plunging cycles. It shows that site 0 and site 2 readings are already outside the test limits, causing these sites to lose yield. Another example where Reg_Vdiode is again tracked (Figure 12). Notice the abrupt changes in the last third of the chart with a sudden deterioration of the temperature reading with a drop on the up to 10% of the yield.

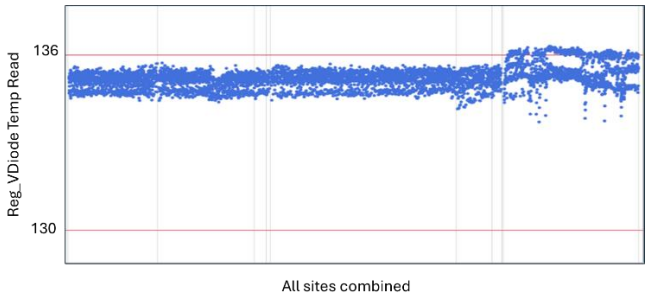

Fig. 12. Bad Reg_Vdiode Temp Read tracking. The figure shows diode temp reading on all sites tracked over time.

With this parameter, we can visualize the behavior of electrical test results with respect to temperature, which would provide us with good insight on how to correct the problem. The handler's ATC control includes a "Temperature Compensation Value" for each site. This compensation value is one of the handler's features that can be adjusted to calibrate the handler's temperature. Adjusting the setting proportionate to how far the device diode temperature reading relative to the nominal shows a significant improvement in the Reg_Vdiode test reading (Figure 13).

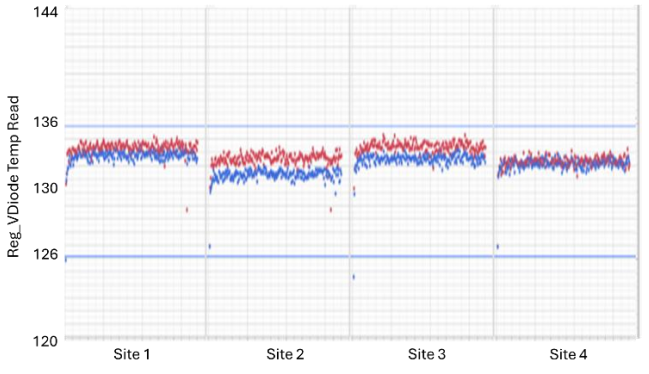

Fig. 13. Good Reg_Vdiode Temp Read. The Figures show good diode temp reading with all sites within the expected temperature range in contrary to the previous fig. 4.

Examination of the downtime records shows that this coincided with a repair activity done on the handler. During the repair, the technician made an error when re-connecting the LN2 hoses, messing up the temperature feedback control on all test sites. Figure 14 below shows how the hose was wrongly connected. The error was later corrected resulting in the restoration of LN2 flow and good diode temperature reading (Figures 15 and 16).

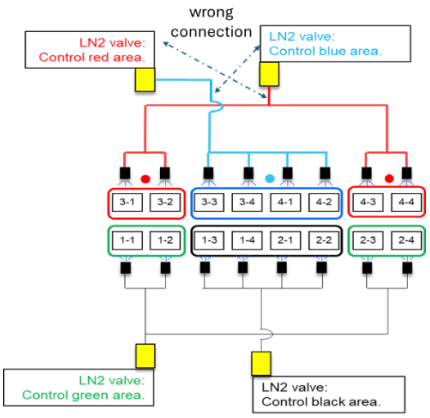

Fig. 14. LN2 schematic with error. The upper LN2 hoses are wrongly connected to the valves.

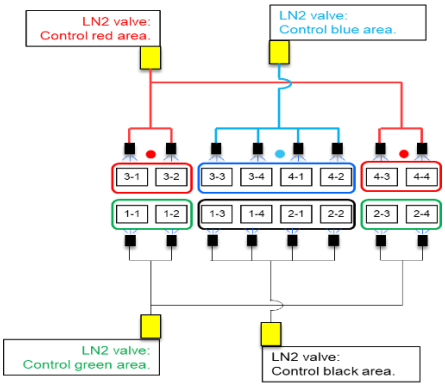

Fig. 15. Correct LN2 schematic. The figure shows the correct connection of hoses to the LN2 valves.

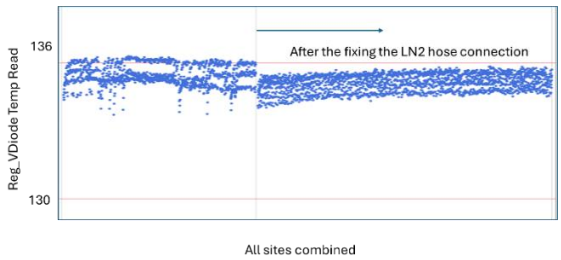

Fig. 16. Good Reg_Vdiode Temp Read tracking. The figure shows diode temp reading after the error the fixing of LN2 hoses.

4.3 Front Arm vs. Rear Arm Reject Clustering detection

If the Front Arm and the Rear Arm test results are left combined, they will appear as one system. As shown below, there are a lot of failures on the RDSON parameter around 21% (Figure 17). The tendency would be to misjudge both arms with bad sites and would lead to troubleshooting through changing of the hardware such the CUH or load board or to running tester diagnostics.

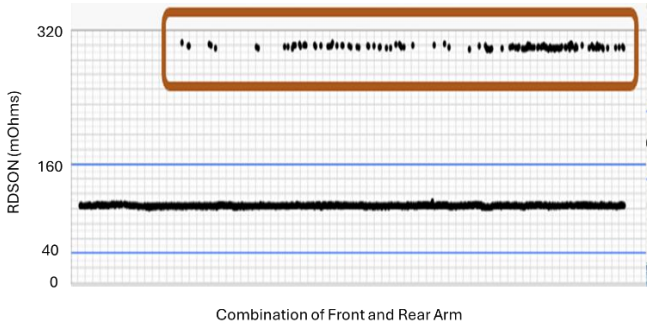

Fig. 17. Combined RDSON Measurements. The figure shows the separation of Front Arm data and Rear Arm data to reveal "clustered rejects."

At one glance, it seems like there is a problem with the setup or the hardware used but it is not. The reality is that the hardware is all fine since they could yield well when the Rear Arm is used. This only becomes apparent when the test results are separated between the Front Arm and the Rear Arm (Figure 6). Apparently, the Front Arm has a problem and will need to be fixed. After fixing the front Arm, the yield significantly improved from 21% to 95%.

The separation of results between the Front and the Rear Arms is done through the additional feature that we added on the current system of the handler. There are three components that were followed on the feature. 1st the Arm Type info (Front or Rear) needs to be appended to the Start-of-Test command from the handler. Next, this Arm Type info must be logged on to the STDF for each plunge cycle and will be included on the system database. 3rd, the data then will be available for download and can now be used for analysis, the Arm Type info must be filtered to show Front or Rear data only.

5.0 CONCLUSION

The three critical setup parameters—Plunger Force, Test Site Temperature, and Front Arm vs. Rear Arm Reject Clustering—play a pivotal role in semiconductor handler performance. Proactive analysis and optimization of these parameters enhance troubleshooting efficiency, expedite identification of suboptimal test sites, and improve overall yield.

Plunger Force: Adjusting this parameter within the optimal range ensures proper contact and stable electrical connections during testing, minimizing false failures.

Test Site Temperature: Precise control of temperature maintains reliable and repeatable test results, especially for temperature-sensitive devices.

Front Arm vs. Rear Arm Reject Clustering: Analyzing reject clustering patterns between the front and rear arms aids in identifying problematic test sites, enabling targeted troubleshooting.

In a pilot run involving over 2 million devices, yield increased remarkably from 25% to 90%. These findings emphasize the importance of monitoring and adjusting setup parameters alongside traditional troubleshooting methods. By leveraging these indicators, semiconductor testing operations can optimize production processes and elevate device quality across Multisite platforms.

6.0 RECOMMENDATIONS

Our current process for measuring setup parametric relies on manual setup and handheld tools, which is both challenging and time-consuming. To streamline data collection, we propose developing a multisite tester-based system that allows simultaneous measurement across Multisite platforms. Additionally, real-time monitoring of Setup parametric information through an online application connected to the tester/handler setup will improve efficiency of data gathering and analysis.

7.0 ACKNOWLEDGMENT

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Obrien "Brix" B. Requina is a dedicated Registered Electrical Engineer with a bachelor's degree in electrical engineering from Central Mindanao University. With over 20 years of experience in the Semiconductor industry working on Electronic and Mechanical hardware design and simulation, he has honed his skills in designing hardware such us test sockets, change kits, docking solutions, etc., and the operation and debugging of roadmap Testers and Handlers. Currently serving as a Principal Product and Test Engineer, he focuses on driving yield improvements, reducing test times, and effectively debugging failures using a variety of state-of-the-art testers and handlers. His expertise extends to automation, robotics, hardware design, simulations, and fabrications, showcasing a versatile skill set that has enriched his professional journey.

Emmanuel "Manny" Mandac graduated from the University of the Philippines with a bachelor's degree in electrical engineering. He has over 40 years of semiconductor test experience and specializes in setup integration, both for wafer probe and handler test. He has extensive knowledge of probers, handlers, docking, probe cards, Loadboards, and sockets. Having spent a lot of years working on prober setups and handler setups, he has gained a lot of insights on how to stabilize production setups.