RISK OF BULK CONTAINERS FOR ELECTROSTATIC DISCHARGE (ESD) ON ESD SENSITIVE DEVICES

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ABSTRACT

Shipping Containers being used during transit of fresh materials from Assembly House to Test Facility plays an important factor in ensuring that the units are intact upon its arrival. It is expected that there would be no yield fall-out that can be induced during transit. However, unnecessary unit movements during transport can generate triboelectric charges that when discharged improperly may result to an Electrostatic Discharge (ESD) event. ESD Sensitive Devices having low ESD ratings (e.g., HBM at 250V) that has no built-in ESD protection cells and with only bypass capacitors as part of its design to operate at high frequency range (5Ghz to 20Ghz) are susceptible to these damages.

This paper will discuss a case study that was performed in identifying the cause, understanding the risk of ESD damage on fresh materials using Bulk Shipping Containers and drive a change on the shipping container to permanently address yield fallouts and reliability risk in a form of walking wounded materials that can reach the customer and equivalently become a quality return.

Figure 1. Sample of Bulk Containers used in shipping (Anti-Static Bag & 2 types of Canisters)

1. 0 INTRODUCTION

The primary driver for the case study is to understand why a certain ESD Sensitive Device that operates as a Power Amplifier at 5-20Ghz frequency with ESD rating of 250V HBM has recurring customer returns due to dielectric rupture on the capacitor caused by an ESD damage. The same damage is also observed on capacitor (CAP) yield fallouts at Test that is captured on parameters related to the capacitor while its co-fab does not.

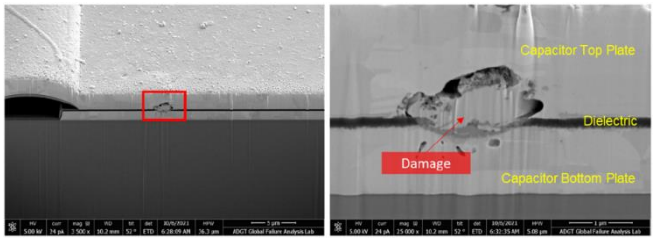

Figure 2. Sample Capacitor ESD-induced Damage on the ESD Sensitive Device

This led to the implementation of increased controls into the production line with examples like from 1x to 3x production testing, porting of the ESDS device to a Class 0 (HBM Voltage Threshold <250V) [1] handler and creation of pre and post CAP parameter into the program to capture latent failures and ensure that only robust parts will be shipped to the customer. The introduction of the added tests to ensure quality resulted to increased test time and lead time for shipping.

Tracing back the Genealogy, it was observed that the same die is assembled into two (2) different assembly houses that ships the fresh material to the test facility via Bulk Container (Anti-Static Bag) or Tube.

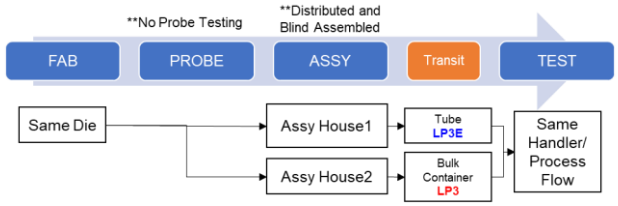

Figure 3. Process Flow Mapping comparison of the Co-Fabs

The study mainly revolves on data collection and proving hypothesis that will focus on the only observable difference on the process flow on the co-fabs which is the shipping medium during transit and will derive recommendations based on the experimentations done.

2. 0 REVIEW OF RELATED WORK

Not Applicable.

3.0 METHODOLOGY

The problem was defined based on the customer return occurrence and the recent processed lots' performance at Final Test, though the 2 Assembly House carries the same die, it can be observed that the LP3E part has significantly lower Cap Fail % (<1%) versus the LP3 part (5-12%).

Assigning matching colors to Lots with the same Fab Lot ID, it can be further deduced that the capacitor failure is not inherent on the die since the distributed materials between the Assembly Houses does not produce the same Cap Fail %.

The Test Facility can also be removed from the possible sources of ESD equation since the Handlers/Fixtures used does not establish commonality and are both used on the LP3E and LP3 parts.

Table 1. 1-Year Span of Customer Return Occurrence and Final Test Processed Lots Data Consolidation

Customer Return Occurrence

LP3E	1
LP3	3

Lots Processed at Final Test

LOT#	Part #	Fab_Lot_ID	Assy_Lot_ID	Board	Tester	Handler	Assy Site	Cap Fail %
1	LP3E	**WP986P181**	5492387.1	P41801001	01RNSAMP	01ISMCPS	Assy House1	0.074%
2	LP3E	WP986P180	5492386.1	P41801002	02RNSAMP	12ISMCPS	Assy House1	0.085%
3	LP3E	WP986P185	5659031.1	P41801001	05RNSAMP	01ISMCPS	Assy House1	0.000%
4	LP3E	WP986P184	5659040.1	P41801005	02RNSAMP	03ISMCPS	Assy House1	0.049%
5	LP3E	**WP986P182**	5641995.1	P41801005	02RNSAMP	03ISMCPS	Assy House1	0.000%
6	LP3E	WP986P183	5659033.1	P41801001	05RNSAMP	01ISMCPS	Assy House1	0.518%
7	LP3E	WP986P184	5659032.1	P41801001	05RNSAMP	01ISMCPS	Assy House1	0.024%
8	LP3	WP986P161	4905856.1	P41801002	02RNSAMP	12ISMCPS	Assy House2	3.093%
9	LP3	WP986P179	5479347.1	P41801002	02RNSAMP	12ISMCPS	Assy House2	12.550%
10	LP3	WP986P179	5479347.1	P41801002	01RNSAMP	06ISMCPS	Assy House2	5.236%
11	LP3	**WP986P181**	5554425.1	P41801001	05RNSAMP	03ISMCPS	Assy House2	4.50%
12	LP3	**WP986P181**	5554425.1	P41801001	02RNSAMP	15ISMCPS	Assy House2	5.004%
13	LP3	**WP986P182**	5625910.1	P41801001	01RNSAMP	01ISMCPS	Assy House2	9.149%

Assembly-wise, the 2 houses conduct similar processes with ESD controls intact upon receipt of the Wafer from Fab up to the Assembled Device for transit to Test. However, the LP3 device transit package is an Anti-Static Bag which is prone to device movement within that could allow unit collision and is susceptible to Triboelectrification or Retained Charges.

Triboelectrification is described as when a device and package move in relation to each other, charge is accumulated on the package and on the device. When the device contacts an object with a different potential, like a grounded work surface, an electrostatic discharge occurs [2].

Furthermore, Retained Charges is explained as the event where the package can gain charge from ESD or triboelectrification where the package exterior is isolated from the package interior and the device. Therefore, it is possible for charge on the package to discharge to the device as it is removed from the package [3].

Hypothesis on the Anti-Static Bag possibly generating retained charges or triboelectrification that could affect the in-transit ESDS device that may damage the capacitor and result to the CAP fallout was further examined by endorsing the actual bag for ESD Checking under ADP00559: Electrostatic Discharge (ESD) Protection Guidelines.

Measurements were done under the Qualification guidelines that considers environmental conditions where the packaging materials will be subjected. For manufacturing materials that are used to process the ESDS devices, only the ambient temperature and relative humidity must be comprehended. For materials that will be part of the ESDS device packaging, qualification measurements must be both on the conditions below [4]:

RH=12%, ±3%; Temp = 23ºC ±3%
(Denotes uncontrolled environmental condition like outside the controlled manufacturing RH and during Transit)

RH=50%, ±5%; Temp = 23ºC ±3%
(Denotes controlled environmental condition which is the Manufacturing Floor)

Table 2. Results showed that the Anti-Static Bag used for transit was failing the uncontrolled environmental condition (RH=12%) that can also be equated to the in-transit condition

			Temperature = 23C +/- 3C Relative Humidity = 12% +/- 3%					Temperature = 23C +/- 3C Relative Humidity = 50% +/-5%				
	Material	Parameter	Temp	RH	Reading	Criteria	Remarks	Temp	RH	Reading	Criteria	Remarks
	Conductive (ASR) Bag	Surface Resistivity Measurement	23.6C	12%	3.8E11 OHMS	>1.0E04 TO <1.0E11 OHMS	FAILED	20.9C	50.1%	1.8E09 OHMS	>1.0E04 TO <1.0E11 OHMS	PASSED
		Static Voltage Reading (Without Tribo Charge)	23.6C	12%	60V	< 100V	FAILED	20.6C	50.1%	5V	< 100V	PASSED
		Static Voltage Reading (With Tribo Charge)	23.6C	12%	650V			20.5C	50.1%	10V		

The ESD testing outcome validated the hypothesis that the Anti-Static Bag contributes to the generation of ESD via retained charge or triboelectrification that could be dissipated into the LP3 device and could damage the capacitor that is directly connected to the external pins. This is equivalently being captured by the CAP parameters at Final Test that results to high yield offs.

With the validated hypothesis, the next step is to generate the corrective actions. Given that the co-fab material that has lesser cap fallouts is using a tube during transit from Assembly to Test Facility, a Special Lot Request (SLR) was created to request from Assy House 2 to still generate LP3 materials to be shipped to Test. But instead of the Anti-Static Bag, a Tube provided by the Test Facility will be used as a transit medium that upon arrival will be tested on the same controls being used on the LP3E part. The conversion to Tube medium is theorized to limit the collision and movement of

the devices, thereby dampening the possible effects of retained charges or triboelectrification that could damage ESDS devices.

The Test results of the LP3 SLR lot using a Tube for transit showed a drastic drop from the typical previous cap fallout of around 5-12% down to 1% which is the same values from the co-fab LP3E devices. This also proves that the assembly processing of LP3 device from Assy House 2 has no contribution on the ESD failures and is narrowed down to the shipping medium used during Transit.

4.0 RESULTS AND DISCUSSION

With this study, /use of scientific approach and design of experiments, the team arrived on the following results:

1) Bulk containers are susceptible to retained charges or triboelectrification through unnecessary movements or collisions that can be discharge to the unit in transit. This was proved during the experimentation where the shipping medium was changed from Anti-Static Bag into a Tube through a Special Lot Request where significant drop was observed on the capacitor fall-out.

2) Derivation and Validation of Hypothesis is a good tool in proving a case study.

3) Materials may have different ESD responses depending on the condition it was subjected to (e.g., Relative Humidity and Temperature).

4) Co-Fab Process Mapping Comparison aids in realization of possible area to narrow down during the investigation

5.0 CONCLUSION

The successful comprehension of the issue at hand led to the acceptance of the Assembly House2 using Bulk Container (Anti-Static Bag) to convert into Tube Output for shipping. Once qualified, the production flow will revert to its normal processing and will permanently address the unwanted capacitor fallouts that can be induced during device transportation.

This study supports the No Good Die Left Behind Initiative where process steps are reviewed to ensure that the process does not introduce or prevent unnecessary fall-outs.

Furthermore, Quality concerns regarding ruptured dielectric on the capacitors due to ESD during transit would be prevented and walking wounded units that could become a quality return will be eliminated.

6.0 RECOMMENDATIONS

With the study and experimentations done to provide evidence on the Risk of Bulk Containers during transits, it is recommended to have a sweep of other possible ESD Sensitive Devices that is still using the same container in shipping the materials to the next processing step.

This is applicable to the manufacturing industry and will further expound the observed risk.

7.0 ACKNOWLEDGMENT

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