REDUCTION OF DIGHSB BOARD FAILURE IN DEVICE "S"

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ABSTRACT

One key part of Automated Test Equipment is the Digitizer High Speed (DIGHSB) Board which converts analog signal into digital signal.

This study aims to reduce or deplete the rampant failure of DIGHSB Board in MOD1 (MODULE 1) area of ams Asia Inc. The process had encountered Gross "Failure X" (Code for defect) in Device S at MOD1 which results to replacement of DIGHSB board of Tester even though board calibration is passing (PCFD – "Passed on Calibration Failed on Device).
There is a recorded 37 occurrences of board failure in 2021 and 30% of overall failed boards are DIGHSB on Device S only.

This has an impact of "$SSSK" loss per year due to shipment and repair cost, yield loss, and production downtime.

DIGHSB Board Failure is at 0% after implementation of the improvements (more than 1 year monitoring). There's no Gross "Failure X" observed as of the moment. All distribution of data are correlated after the new revision of test program and grounding poka yoke improvements were implemented. DMAIC (Define, Measure, Analyze, Improve, and Control) Methodology had been an effective problem solving tool to find the real root cause and effective solution to the problem.

1. 0 INTRODUCTION

1.1 Project Problem Statement

Frequent Gross "Failure X" in Device S at MOD1 results to replacement of DIGHSB board. (37 occurrence on 2021. 30.58% of overall failed boards are DIGHSB on Device S only). Shipment and repair cost of "$SSSK" per year and a total output loss of 600K/ year.

1.1.1 Project Scope/ Limitations

This project will only cover the reduction of "Failure X" which causes the defective DIGHSB board of the Tester for Device S.

1.1.2 Project Goals and Targets

The goal of the project is to reduce the defective DIGHSB board by 70% per quarter (1 occurrence only per quarter) by Q1'2022. It aims to reduce the Gross "Failure X" Yield Loss by 50% and improve the Cpk by minimum 1.33.

2. 0 REVIEW OF RELATED WORK

Not applicable.

3.0 METHODOLOGY

3.1 Define Phase

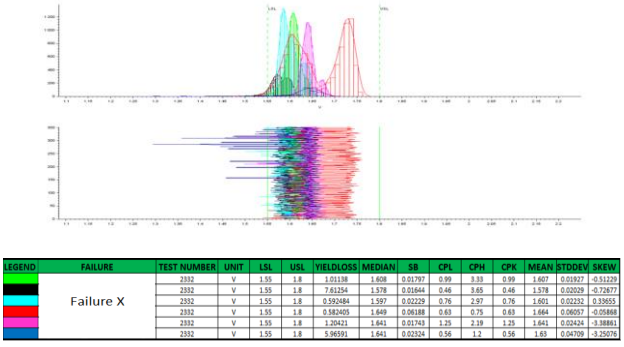
Project Problem Statement: There were 37pcs. defective DIGHSB Boards for 2021 due to encountered rampant "Failure X". 30.58% of overall failed boards for "Device S" only.
"Failure X" accounts for 0.028% with average Cpk of 0.78 only.
This problem results to xx$ losses due to board shipment and repair cost, and yield and output losses of 600K/year.

"Device S" is the pilot device. This project covers the reduction of "Failure X".

Project Risk: Monitor the critical parameters that might be affected due to the improvement and possible changes on Hardware and Software.

3.2 Measure Phase

Process Performance



LEGEND	FAILURE	TEST NUMBER	UNIT	LSL	USL	YIELDLOSS	MEDIAN	SB	CPL	CPH	CPK	MEAN	STDDEV	SKEW
	Failure X	2332	V	1.55	1.8	1.01138	1.608	0.01797	0.99	3.33	0.99	1.607	0.01927	-0.51229
		2332	V	1.55	1.8	7.61254	1.578	0.01644	0.46	3.65	0.46	1.578	0.02029	-0.72677
		2332	V	1.55	1.8	0.592484	1.597	0.02229	0.76	2.97	0.76	1.601	0.02232	0.33655
		2332	V	1.55	1.8	0.582405	1.649	0.06188	0.63	0.75	0.63	1.664	0.06057	-0.05868
		2332	V	1.55	1.8	1.20421	1.641	0.01743	1.25	2.19	1.25	1.641	0.02424	-3.38861
		2332	V	1.55	1.8	5.96591	1.641	0.02324	0.56	1.2	0.56	1.63	0.04709	-3.25076

Fig. 1. Above shows the current Process Performance.

The data shows the process performance of different lots that manifested the Gross "Failure X". Based on the graphical presentation, the process is out of control which is why this is the reason that DIGHSB board of different test systems becomes defective. The data is right skewed which indicates that the process is not good.

3.3 Analyze Phase

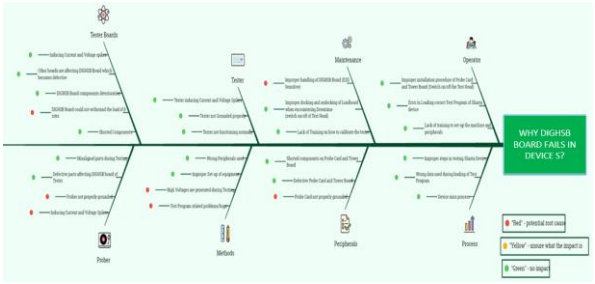


Fig. 2. Ishikawa or Fishbone Diagram

Above is the Ishikawa or Fishbone Diagram that identifies the possible root-causes of the problem. Potential culprit of the problems are Improper handling of DIGHSB Board - ESD (Electrostatic Discharge) Sensitive, DIGHSB Board could not withstand the load of 8 sites, Prober not properly grounded, Prober inducing Current and Voltage Spikes, High Voltages are generated during Testing, Test Program related problems/bugs and Probe Card not properly grounded.

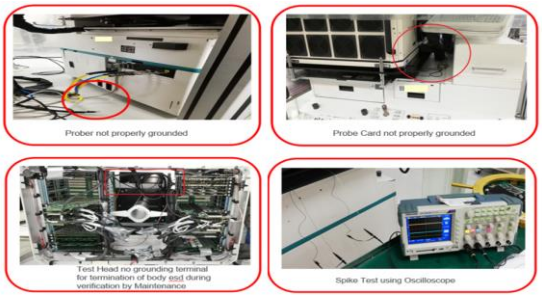


Fig. 3. Potential root-causes of the Problem

Root-causes of the Problem were identified thru Gemba Walk, Observation and Analysis at the line.

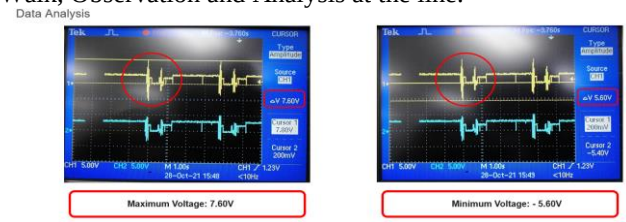


Fig. 4. Data Analysis using Oscilloscope

The data shows the Spike Test of Voltage using Oscilloscope. The Yellow signal is from sites 1-4 and the Blue Signal is from sites 5-8. It indicates that Bin 7 or Reject unit has Maximum Voltage of 7.6V and Minimum Voltage of - 5.6V in a single test. This resulted to Gross "Failure X". DIGHSB Board becomes defective and has been replaced to make the set-up okay and available for testing.

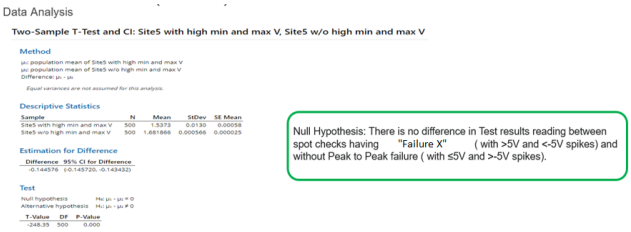


Fig. 5. Data Analysis using Two-Sample T-Test

Using Two-sample T-Test, Null hypothesis is rejected because P-Value is less than 0.05.
It was observed that there is a difference in Test Result Readings between spot checks having "Failure X" and without "Failure X".

Summary: The "Red" X

High Voltage Spike in a single test makes the DIGHSB Board Defective

It was identified by the Team that the culprit of the problem are High Voltage Spikes generated on single test. This makes the DIGHSB Board Defective.

3.4 Improve Phase

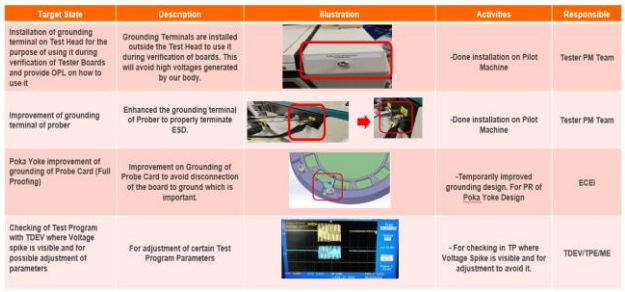


Fig. 6. Brainstorming of the Team for Solutions

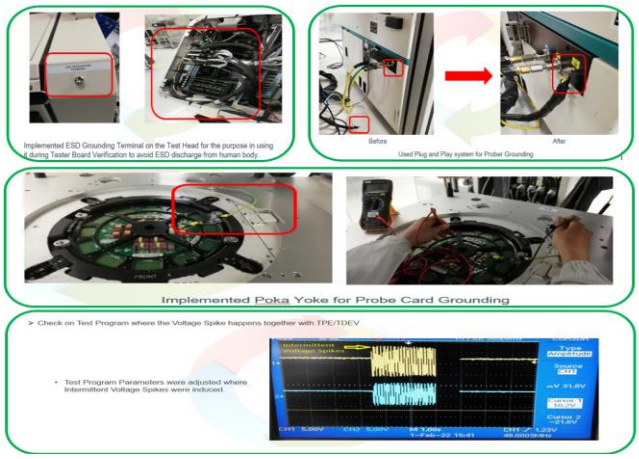


Fig. 7. Description of Target State of Solutions

Above are the solutions implemented to address the Voltage Spikes problem. The main solution is optimization of the test program where the voltage spikes happens. Other grounding solutions were implemented for mistake proofing.

3.5 Control Phase

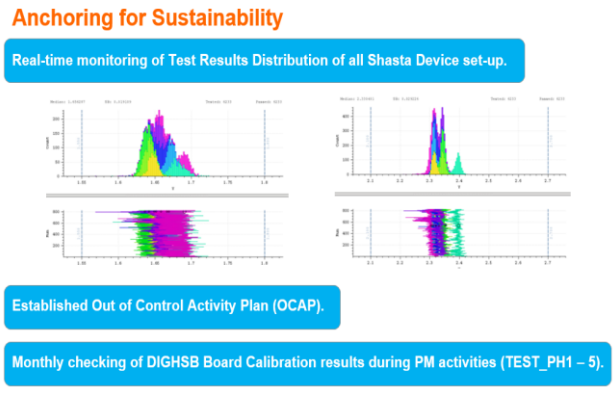


Fig. 8. Anchoring for Sustainability of the Solutions

4.0 RESULTS AND DISCUSSION

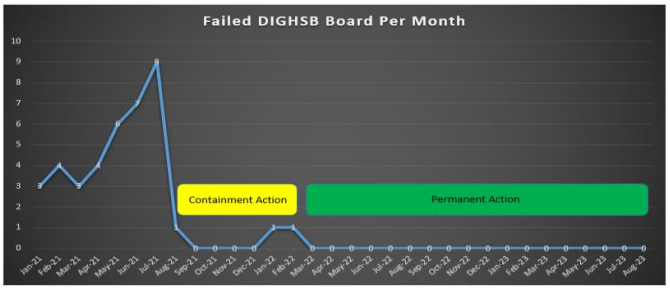


Fig. 9. Trend Chart of DIGHSB Board Failure

Based on the pilot run of all solutions, the target of 70% reduction of defective DIGHSB Board is achieved. Zero board failure has been achieved from March 2022 to August 2023.

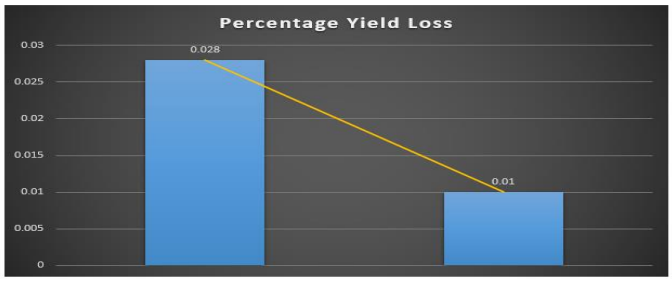


Fig. 10. Percentage Yield Loss

Percentage Failure X was lessened from 0.028% to 0.01%.

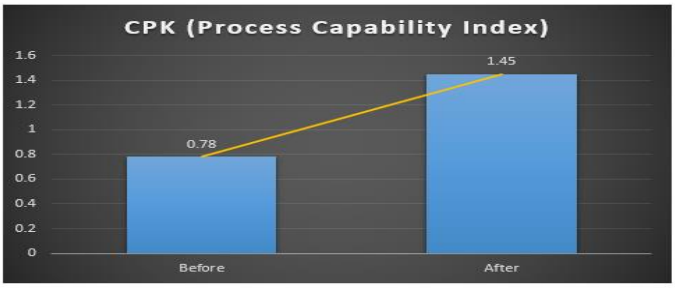


Fig. 11. Process Capability

After the implementation of the solution, CPK (Process Capability Index) has improved from an average of roughly 0.78 to 1.45

5.0 CONCLUSION

It can therefore be concluded that the analysis and the solutions implemented (parameter optimization and poka yoke solution) have been effective to bring down the cost of

shipment and repair, downtime and output losses. Yield Loss was reduced significantly to 0.01% from 0.028% and the CPK has improved from 0.78 to 1.45. The project has brought significant cost savings to the company.

6.0 RECOMMENDATIONS

Based on the analysis of the problem, the main culprit is the voltage spikes that enters the main circuitry of DIGHSB Board. It is recommended for this kind of situation to always check the Test Program along with Spike Test in order to identify the main root-cause. For further studies, electronic components could also be considered for the integrity of the circuits to avoid such spikes.

7.0 ACKNOWLEDGMENT

The success of this project acknowledges all of the team members who helped to solve the problem. First is the Tester Preventive Maintenance Team who focuses on the isolation of defective boards and finding the root-cause. Then Test Product Engineering and Test Development Engineering Team for helping to find the problem on Test Program. Last but not the least is the Lean Team who has shared the knowledge about Six Sigma to solve every difficult problems methodologically.

8.0 REFERENCES

"TESTER S" PREVENTIVE MAINTENANCE AND CALIBRATION PROCEDURE, TEST_PH1 – 5, Specification Document

9.0 ABOUT THE AUTHORS

Jasten S. Duremdez is a graduate of University of Batangas with a course of Bachelor of Science in Computer Engineering. He is currently working as a Staff Test Maintenance Engineer at ams OSRAM Group.

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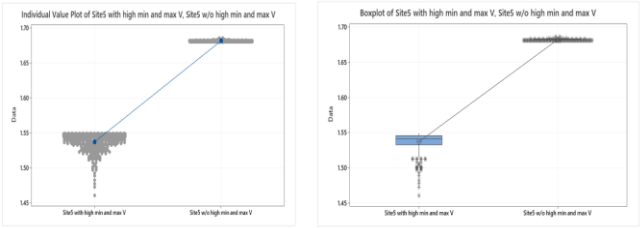
Philip G. Bullas is a graduate of University of Batangas with a course of Bachelor of Science in Computer Engineering. He is currently working as a Staff Test Maintenance Engineer at ams OSRAM Group.

10.0 APPENDIX

APPENDIX A.

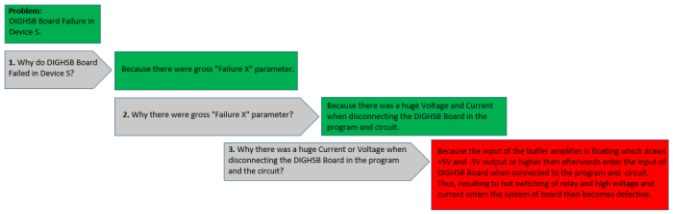


The box plot above shows the spot check done with 500 samples of Test results reading. It was a comparison between the reading with high voltage spikes (minimum and maximum) versus the low voltage spikes. This was taken on single site only where "Failure X" was rampant or gross.

APPENDIX B.

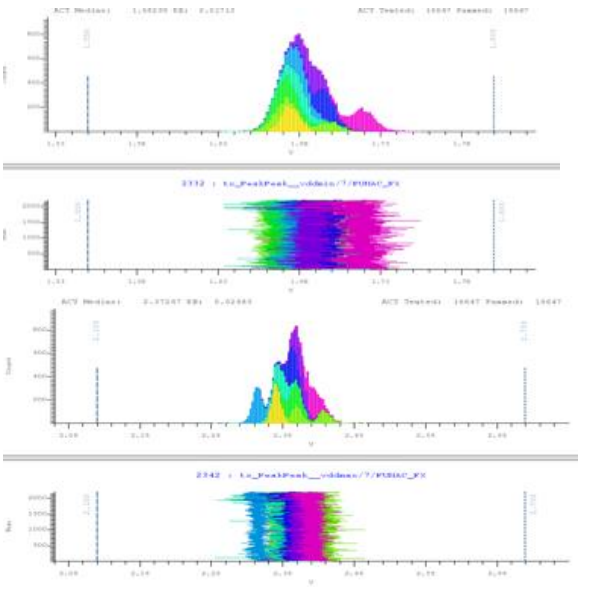
The Histogram above shows the actual "Failure X" that is common to site 5 only. This happened in MXxx last October 28, 2021. After replacement of DIGHSB board, the set-up meets the specifications.

APPENDIX C.



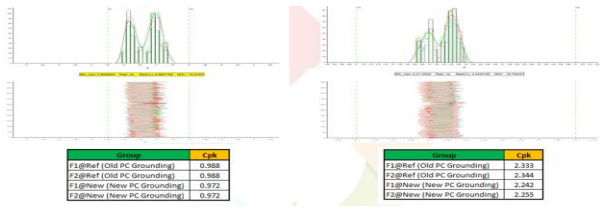
The diagram shows the why why analysis for the identification of the root cause of the problem.

APPENDIX D.



Good Sample distribution of Data after the Test Program Revision.

APPENDIX E.



Gross	Cpk
F1@Ref (Old PC Grounding)	0.988
F2@Ref (Old PC Grounding)	0.988
F1@New (New PC Grounding)	0.972
F2@New (New PC Grounding)	0.972

Gross	Cpk
F1@Ref (Old PC Grounding)	2.333
F2@Ref (Old PC Grounding)	2.344
F1@New (New PC Grounding)	2.242
F2@New (New PC Grounding)	2.255

After the implementation of grounding improvements, Distribution on Gross “Failure X” parameters are correlated (Before and After).