TITLE (REDUCTION OF IGBT SIDE WALL CRACK)

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ABSTRACT

Dicing or wafer saw is a major process that every single integrated circuit chip goes through. This is the process wherein individual die of a semiconductor wafer is separated from each other. Today, there are different technologies used in dicing process but mechanical dicing using diamond blades remains to be the most cost-effective method. Common quality issues at dicing process are surface chipping and backside chipping. But with the introduction of new wafer technologies, other quality issues became critical. One of these new critical quality issues is the side wall crack.

This paper focuses on understanding the different causes of side wall crack in IGBT wafer. Aside from dicing process, die bond process was also scoped in this paper since these two processes have high interaction. After understanding and validating the root causes, improvement actions were formulated to reduce the occurrence of side wall crack. Design of experiments (DOE) was performed to determine the best dicing parameters and conditions. The critical factors included were diamond blade, cutting speed and cutting height ratio. Die bond machine pick-up parameters and expansion level were also optimized. Since side wall crack cannot be seen after dicing process, it is being monitored after die bond process through manual angular inspection. Other factors such as dicing tape, cutting sequence and blade dressing were also explored in this paper.

After implementing the optimized parameters and conditions, the overall IGBT sidewall crack ppm significantly improved from 1466ppm to 0 ppm. Manual angular inspection, which was considered a non-value-added activity, was eliminated. It is hoped that this paper will help the technical society in the semiconductor industry to better understand side wall crack occurrence and the different ways to address them.

1. 0 INTRODUCTION

Side wall crack is a line at the side wall of die along which it has split without breaking into separate parts. It is a type of defect that occurs when the die is subjected to unwanted force or stress.

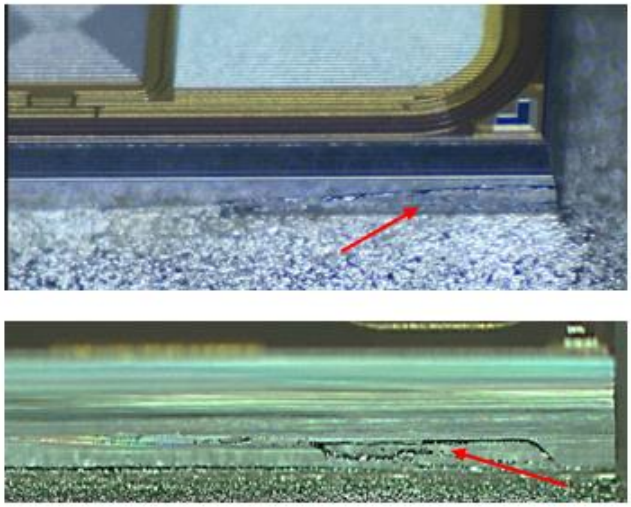

Fig. 1. Side Wall Crack

Dicing of IGBT wafers is challenging because these wafers have PN junction along the side wall. This PN junction is critical and must not have any cracks or chipping. Any damage to the PN junction will cause electrical failure.

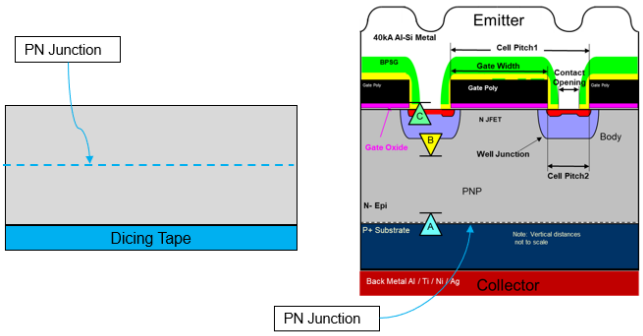

Fig. 2. IGBT Structure

The main objective is to reduce the side wall crack ppm level from 1492 ppm to 400 ppm by Apr 2023. The defect ppm baseline was derived from Nov-Dec 2022 only since these are the months covered by the increase sampling inspection at die bond process.

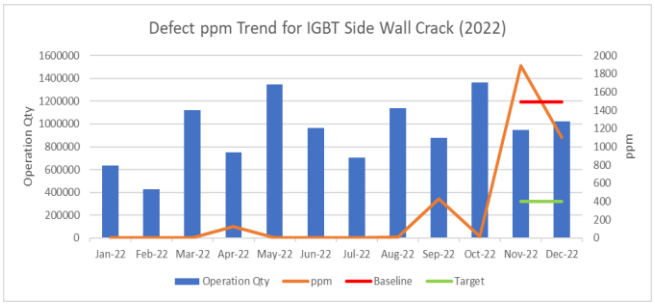

Fig. 3. IGBT Side wall crack defect ppm trend

2. 0 REVIEW OF RELATED WORK

No external related studies were reviewed during the course of this project.

3.0 METHODOLOGY

In order to determine the possible root causes of side wall crack and side wall chipping, fish bone analysis was used. The possible root causes identified were:

- Insufficient blade interval dressing
- Not optimized dicing parameter
- Not optimized pick-up parameters
- Machine mechanical limitation of the DB expander
- Inappropriate Blade thickness used

3.1 Validation for Insufficient blade interval dressing

When chipping remnants are found on the wafer carcass, side wall crack defects are also seen on the bonded units. The backside coat of IGBT wafers is a ductile material and can easily load the dicing blade. This blade loading hinders the blade cutting ability which leads to chipping and side wall crack.

Fig. 4. Chipping remnants on wafer carcass

Hypothesis test was performed to compare the responses of 2 different blade dressing intervals.

Wafer Carcass Inspection	Z2 BLADE DRESSING FREQUENCY	
	Before	After
	Once per wafer	Twice per wafer (once per channel)
Wafer #1	No chipping remnant seen	No chipping remnant seen
Wafer #2	With chipping remanant seen	No chipping remnant seen
Wafer #3	No chipping remnant seen	No chipping remnant seen
Wafer #4	No chipping remnant seen	No chipping remnant seen
Wafer #5	With chipping remanant seen	No chipping remnant seen
Wafer #6	With chipping remanant seen	No chipping remnant seen
Wafer #7	With chipping remanant seen	No chipping remnant seen
Wafer #8	With chipping remanant seen	No chipping remnant seen
Wafer #9	No chipping remnant seen	No chipping remnant seen
Wafer #10	No chipping remnant seen	No chipping remnant seen

Fig. 5. Blade dressing interval comparison

Based on 20-wafer validation, interval blade dressing of twice per wafer is better than once per wafer since no chipping remnants were found on the wafer carcasses. Chi Squared test was also performed to statistically compare the difference and it is concluded that twice per wafer blade dressing for Z2 is significantly better in terms of side wall crack occurrence.

Test Plan	Chi-Squared Test
Sample Size	20 wafers
Hypothesis Statement	*Ho* : $SWC_{before} = SWC_{after}$ *Ha* : $SWC_{before} \neq SWC_{after}$
Test Result	p-value = 0.0098
Statistical Conclusion	Since p-value <0.05, Accept Ha @ 95% confidence level
Practical Conclusion	Twice per wafer blade dressing for Z2 is significantly better in terms of SWC occurrence.

Condition	Z2 blade dressing
Before	Once per wafer
After	Twice per wafer

Fig. 6. Chi Squared test for blade dressing interval comparison

3.2 CAPA for Insufficient blade interval dressing

Dicing recipe was updated to implement the interval blade dressing. The twice per wafer interval was set for the Z2 blade.

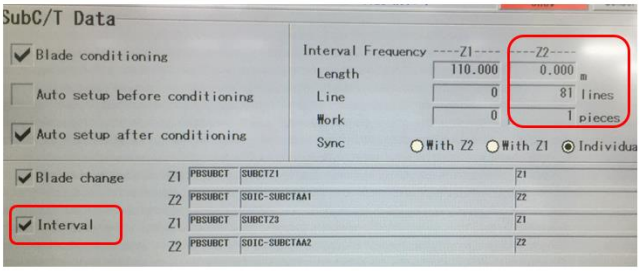

Fig. 7. Interval blade dressing settings (Twice per wafer)

3.3 Validation for Not optimized dicing parameter

DOE was conducted to determine the best dicing parameters. A full-factorial DOE design was used. The identified factors were cut ratio, cutting speed (1st CH) and cut sequence. The monitored response was side wall crack.

Design of Experiment (DOE) PLAN

[Characterization / Optimization]

Study #	
Date	
Pass/Fail	
Process	
Equip	
Start	
Finish	
Page	of

Problem Statement

Not optimized dicing parameter will cause side wall crack.

Objectives

1.Find which factors are significant
2. Find the best combination of the significant factors that will give minimum SWC

Variables Under Study

Dependent Variable(s) (Response)	Data Modelling Type	Number of Replicates	Specification	Unit of Measurement
Side Wall Crack	Continouos	1 wafer per run 10 dice per wafer	<85	um

Independent Variable(s) (Factor)	Data Modelling Type	Number of Levels	Levels	Unit of Measurement
Cut Ratio	Discrete	2	(60/40)/(70/30)	NA
Feed Speed (1st CH)	Discrete	2	20/30	mm/s
Cut Sequence	Discrete	2	2CH/4CH	NA

Experimental Design/Model

Full Factorial

No. of Center Points

None

Fig. 8. DOE Plan

After the DOE validation runs, Cut Ratio, Cut Sequence and Feed Speed (1st CH) and their interactions are significant dicing parameters in the occurrence of SWC. All these factors were used in finding the optimum dicing condition.

3.4 CAPA for Not optimized dicing parameter

The second part of the DOE is the optimization or getting the refined model. The best dicing parameter settings to give the best response in terms of side wall crack are below:

- Cut Ratio: 70/30
- Cut Sequence: 4-Channel Sequence
- Feed Speed (1st CH): 30 mm/s

The best parameters were used on a 30-sample validation run. All side wall crack measurements are well within the specs limit of 85 um and have a Ppk of 2.289.

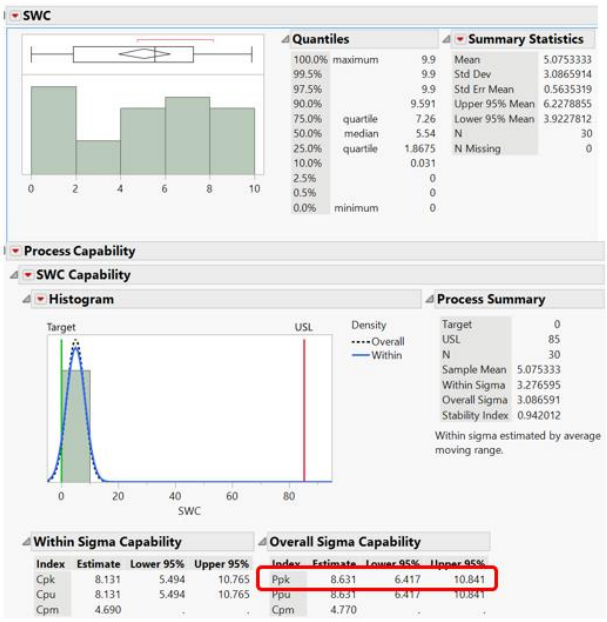

Fig. 9. Side wall crack capability using best dicing parameters.

3.5 Validation for Not optimized pick-up parameters

There are 2 forces acting on the die during the pick-up at die bond process. The downward force of the metal collet and the upward force of the pin. If these forces are not precisely timed, it can create corner chipping and crack. Actual validation was done in the process and this will lead to corner chipping and side wall crack.

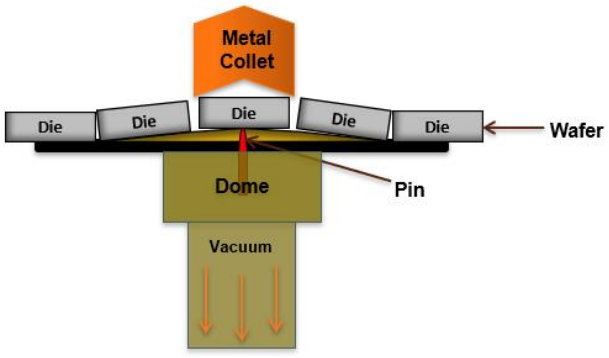

Fig. 10. Die pick-up illustration at Die Bond process

3.6 CAPA for Not optimized pick-up parameters

Sync Pick Mode was enabled in the DB machines.
Sync pick mode settings were optimized to prevent die collision during die pick-up.

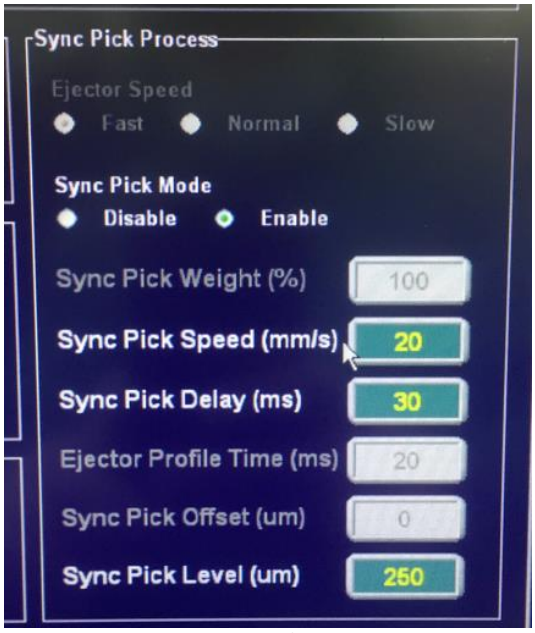

Fig. 11. Sync Pick mode setting for Die Bond machine

3.7 Validation for Machine mechanical limitation of the DB expander

The die bond machine model being used has fixed wafer expansion level and no current way to increase the expansion and die to die clearance. The affected wafers are narrow saw street and use thinner blade which makes the die-to-die clearance smaller. Small die-to-die clearance means higher risk of die-to-die collision. This leads to corner chipping and side wall crack.

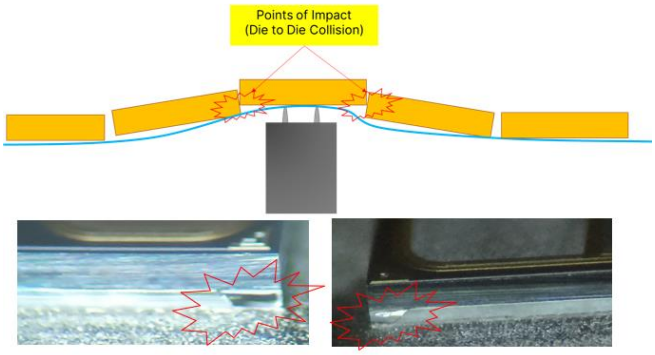

Fig. 12. Die to die collision leading to side wall crack/ chipping

3.8 CAPA for Machine mechanical limitation of the DB expander

The wafer expander of DB machine was modified. A spacer was added in order to increase the expansion of the wafer. This resulted in a wider die-to-die clearance which prevented the die-to-die collision.

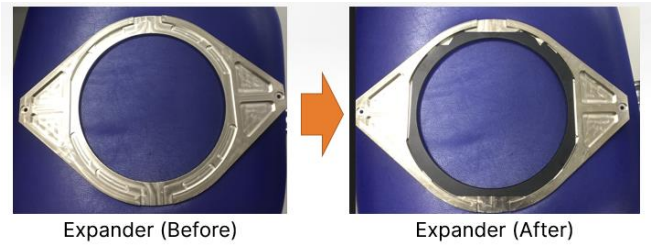

Fig. 12. Die Bond machine expander

3.9 Validation for Inappropriate Blade thickness used

The dicing cut method being used is Step Cut. This method uses two different blades with different thickness. The current minimum blade thickness gap is 5um only.

	Blade Name	Blade Thickness Specs	Minimum Blade Thickness Gap	Minimum Blade Thickness Gap
Z1	Blade A	30-35 um	5 um (2.5 um each side)	15 um (7.5 um each side)
Z2	Blade B	20-25 um		

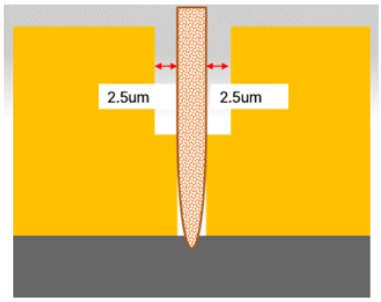

Fig. 13. Current blade thickness gap

This gap does not provide a safe margin for offsetting of the Z2 cut. An offset of >2um on one side will create a NG step cut profile which will lead to side wall crack.

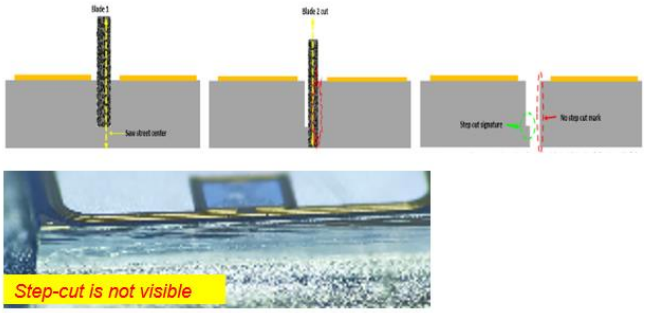

Fig. 14. Failure mechanism for insufficient blade thickness gap.

3.10 CAPA for Inappropriate Blade thickness used

A new thinner Z2 blade was implemented to have a wider blade thickness gap. The minimum gap was improved from 5 um to 10 um.

	Blade Name	Blade Thickness Specs	Minimum Blade Thickness Gap	Maximum Blade Thickness Gap
Z1	Blade A	30-35 um	10 um (5 um each side)	20 um (10 um each side)
Z2	Blade B	15-20 um		

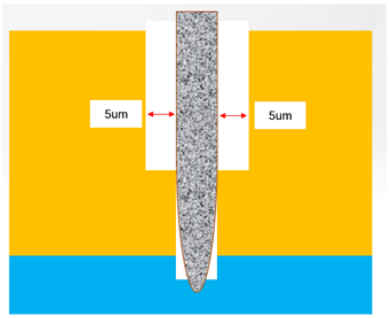

Fig. 14. New blade thickness gap

4.0 RESULTS AND DISCUSSION

After the completion of all the CAPA, the side wall crack ppm has exceeded the goal of <400 ppm and was eliminated.

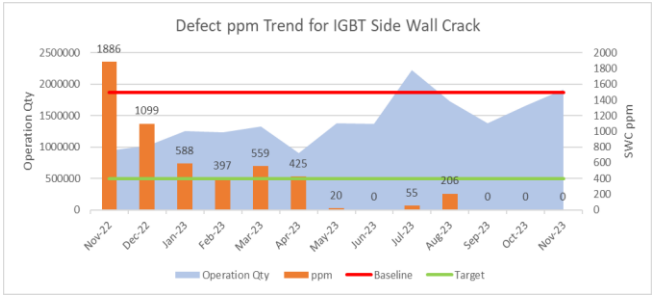

Fig. 15. IGBT side wall crack defect ppm trend after CAPA completion

Lot rejection rate (LRR) at die bond process was also improved by eliminating lots that need to undergo 100% manual angular inspection.

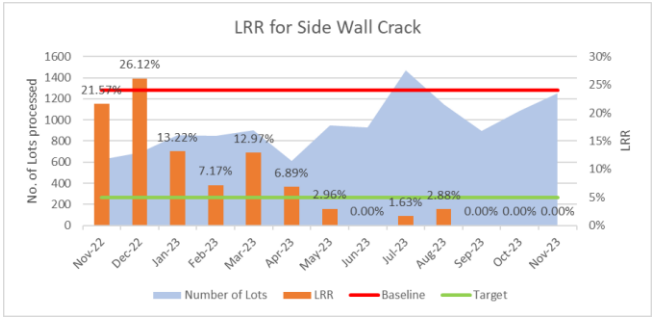

Fig. 16. IGBT side wall crack % LRR at Die Bond process

All actions and controls were documented through forms, work instructions, PFMEA and Control Plan.

5.0 CONCLUSION

The project effectively addressed the side wall crack defects both at dicing and die bond processes. Productivity was also significantly improved upon the elimination of the manual inspection after die bond process. Using Lean Six Sigma (DMAIC) approach in solving issues scoping two or more processes is highly effective. This method also promotes collaboration and creativity which is very beneficial in the semiconductor industry.

6.0 RECOMMENDATIONS

It is highly recommended to fan out the improvement actions to other wafer technologies besides IGBT.

7.0 ACKNOWLEDGMENT

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Mentors: Louie Dizon
Project Sponsor: Joel Medina
Project Champion: Arnel Hulipas
Team Members: Teodorico Benjie Cabailo, Jose Rivera and Mart Candelaria

8.0 REFERENCES

N/A

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10.0 APPENDIX

N/A