PROBE DAMAGE REDUCTION USING KAIZEN METHODOLOGY

Victoria H. Acasio
Michael Angelo N. Carlos
Milyn O. Embang

Probe Department – Production and Engineering
Allegro MicroSystems Philippines, Inc. 4756 Sampaguita St., Marimar Village 1, Sun Valley, Parañaque City
vacasio@allegromicro.com, mcarlos@allegromicro.com, membang@allegromicro.com

ABSTRACT

Wafer Probe is a process where die is tested electrically in its wafer form. To test the wafer, a complete setup is needed such as prober, tester, and hardware. During probe testing, wafers are placed on top of a table called chuck which is to be probed by a probe card. Probe card has pin needles that will contact or touch the die of the wafer (see Figure 1).

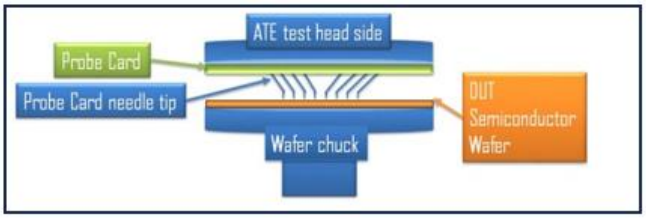

Figure 1. Wafer Probe Testing concept. Wafer placed on top of the wafer chuck. The chuck goes up touching the Probe card needle tip making contact to the wafer called probing.

During wafer testing there are possible defects that can be produced by the process. Among all other defects, Probe Damage can be induced. This is an event wherein a part of die passivation specifically at the pad area has been damaged by probe needle during wafer probing.

Visually the product would manifest its probe mark touching the bond pad boarder area which could expose the base metal (see Figure 2).

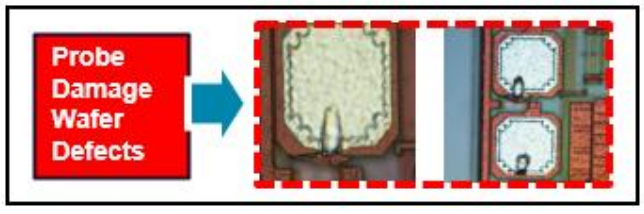

Figure 2. Reject probe marks that exposes oxide beneath the bond pad metal.

For the criteria, the good and acceptable probe marks must be inside or within the bond pad and or as much as possible at the center of bond pad as optimal setting (see Figure 3).

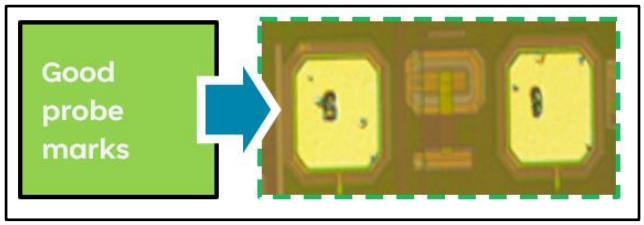

Figure 3. Good and Acceptable probe marks inside the bond pads.

Throughout the study, the team has seen issues coming from Probe Damage being the top contributor of wafer defect induced during probing is at HOT temperature which is averaging at 405 ppm (parts per million).

The team uses different methodologies in identifying the root cause of probe damage. Started using Process mapping to identify the possible source of event of probe damage. Drilling further, the team uses Fishbone to visualize the categories of the potential causes of the problem. Upon determination of the possible root cause, the team performed hypothesis testing for the validations. These tools served as fundamental baseline for accurate root cause analysis to provide effective improvement actions.

From each valid cause of probe damaged the team implemented corresponding corrective actions, which significantly reduced probe damage at HOT setup by 71% from 405 ppm to 117 ppm. With these positive results, the team recommended it to fan-out the learnings that was attained during the course of this project.

1. 0 INTRODUCTION

1.1 Background of the Study

Allegro MicroSystems Phils., Inc. (AMPI) aims to deliver high quality products with Zero Defects which drives the team for continuous improvement.

The Visual Wafer defects at Probe are increasing due to probe damage averaging at 670 ppm per month for Q1 to Q2 Fiscal year 2023. As this defect impacts the productivity and yield, the team investigated to identify the factors causing the probe wafer defects.

There are different kinds of wafer defects in the Probe area such as defective bond pads, cracks, foreign material, burn marks, passivation, fluorine flower, probe damage, smeared metal, punch through, die anomaly, no marks and peeled off streets but the % contribution of the listed defects is low.

Through LEAN tools and techniques, the Probe operations created a team to identify the factors that are contributing to the increase of wafer defects.

Focusing on the wafer defect level, first level pareto analysis shows that the top contributor is Probe Damage with a total of 395k units or equivalent to 68% of total defect from Q1 to Q2 FY23 (see Figure 4).

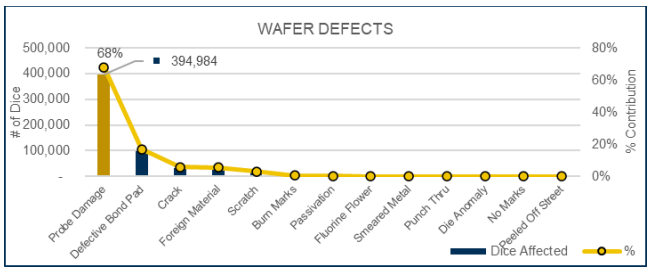

Figure 4. Probe Damage is the top wafer defect.

On second level analysis, the team focused on device resource levels (Resource 1, Resource 2, Resource 3) and the high occurrence of probe damage is coming from Resource 1 resource with a total of 239k die affected or 61% contribution of the total probe damage defect of the same period and is equivalent to 405 ppm (see Figure 5).

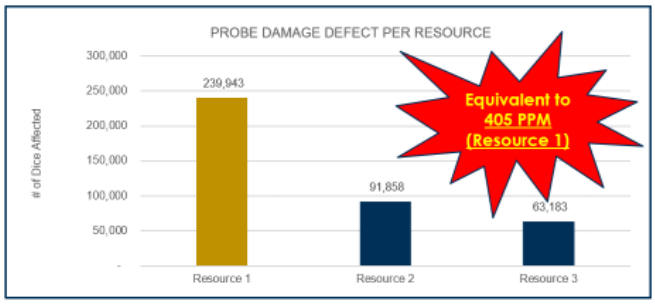

Figure 5. The top resource is Resource 1 with probe damage.

Examining further, on the third level analysis, contribution of the probe card vendor and device level tested at Resource 1 resource was analyzed.

The top probe card vendor inducing high defect of Resource 1 is Vendor A with equivalent of 210k die or 88% contribution from 239k die affected (see Figure 6).

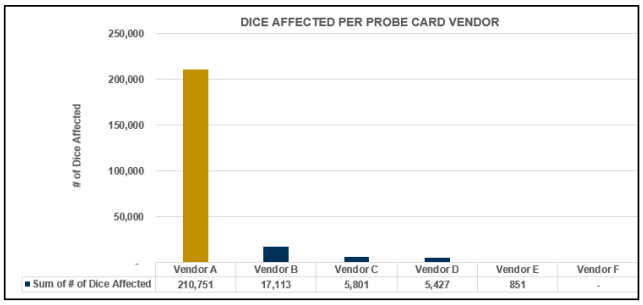

Figure 6. The top source is Vendor A probe card vendor.

The top device producing high defects of Resource 1 is Device 1 with a total of 135k die or 56% contribution of 239k die affected of probe damage and equivalent to 777 ppm with 174k PHP scrap value (see Figure 7). Based on the device pareto of probe damage, all devices affected are all tested at HOT process.

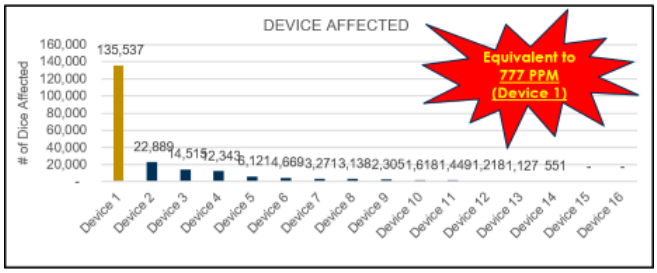

Figure 7. The top device with probe damage is Device 1

To summarize, the team's analysis shows that the top wafer defect is Probe Damage, and its top source is Resource 1. The top contributor of probe damage in Resource 1 is Device 1 using Vendor A probe card which is the major cause of the problem tested at HOT process.

By Probe process mapping and Fishbone Diagram (see Figure 8) the team identified possible root causes of probe damage. From the identified root causes, the team performed validation testing plan (see Figure 9) to confirm the hypothesis. Among the validated processes, the top contributors of wafer defect probe damage are: 1) No probe pin alignment on every wafer; 2) Excessive running overdrive setting; 3) Marginally passing probe mark alignment; 4) Defective epoxy; 5) Vibration from generator.

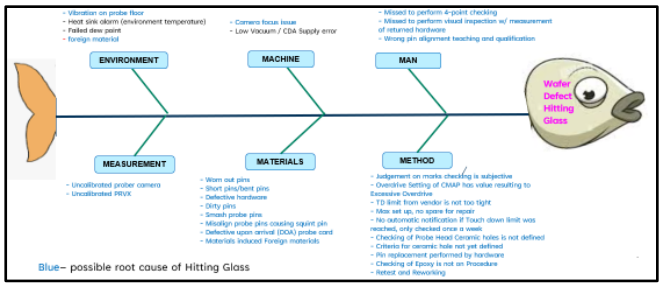

Figure 8. Fish bone diagram identified contributor of probe damage. The items in blue font are the possible root cause.

HYPOTHESIS VALIDATION

Item	Primary Contributing Factors		Secondary Contributing Factors	Control or Action	5Ms Valid Contributors to Hitting Glass (5 out of 9)	Conclusion
1	Lot Preparation	1.1	N/A	N/A		Not Possible
2	Electrical Probe Testing	2.1	No probe pin alignment on every wafer	1. Perform pin alignment for HOT testing devices 2. Simulate for Celadon card tray – molybdenum and non-molybdenum using 25 dice		Possible
		2.2	Excessive Running Overdrive setting	1. Reiterate to all technicians and Optech regarding OD settings 2. Revisit all cmap and OD must be 0 value during cmap download 3.Password protec, access to be given to PE SUS and Supervisors only (Long Term Action)		Possible
		2.3	Marginally passing Probe Mark Alignment	1. Introduce and simulate probe mark alignment template		Possible
		2.4	Defective Epoxy	1. Simulate checking of epoxy during pin repair 2. Include into Probecard PM procedure and additional check items regarding Epoxy crack		Possible
		2.5	Vibration from generator	1. Stop testing the machine 2. Include on OCAP		Possible
		2.6	Preheat not performed (300secs)	1. Simulate cancel preheat 2. Password protec, access to be given to PE SUS and Supervisors only (Long Term Action)		Not Possible
		2.7	Multiple touchdown due to reprobe	1. Check all history of hitting glass. No root cause or findings that hitting glass was caused by multipass 2. Create criteria of reprobe		Not Possible
		2.8	Wrong Polisher Setting	1. Validate if polisher OD will induce needle misalignment 2. Increase polisher OD to 75um for 25 dice		Not Possible
		2.9	Accidental bumping of prober	1. Check probemarks after bumping the prober		Not Possible
3	Evaluation	3.1	N/A	N/A		Not Possible
4	Pack	4.1	N/A	N/A		Not Possible
5	Ship to Die bank	5.1	N/A	N/A		Not Possible

Figure 9. Hypothesis Validation of Possible Root cause of probe damage.

1.2 Objective

The team aimed to reduce the rate of wafer probe damage defect on HOT testing setup cards with Device 1 as lead vehicle by 38% from 777 ppm to 476 ppm (Die Level) by Q4FY23.

The second objective is to reduce the wafer defect at Resource 1 by 50% from 405 ppm to 204 ppm.

1.3 Scope and Limitation

The project focused and simulated on one Prober with running Device 1 target at Resource 1.

2.0 REVIEW OF RELATED WORK – NOT APPLICABLE

3.0 METHODOLOGY

To determine the root cause of wafer defects and areas for improvement and reduce probe damage, the team applied Lean tools and techniques. Starting with Gemba Walk to witness and familiarize the actual process flow versus on the documented procedure, then proceeded to Brainstorming to share observations which built stronger relationships and trust with the team members so that they can share their ideas freely and work together to solve the problems. Along with these, the team completed Process mapping that focused and worked on areas that were seen to be possible cause of wafer defect probe damage. Through the data gathered from relevant resources such as Operators, Supervisors, and Support in production line, the team started to identify the problem and root source using Fishbone Diagram and Hypothesis testing validation. After confirmation, solutions were applied and started the monitoring for the impact of improvements.

The root cause analysis and improvement implemented based on the collected information and validation performed by the team will be explained in the succeeding paragraph.

3.1 Misaligned Probe mark after every change of wafer for hot testing

During investigation, the signature of occurrence happens in every start or change of wafer. Defect manifested on a sudden shift of whole pad probe mark alignment on all probe pads. The team examined the behavior of process and referred to the equipment manuals for reoccurrence of problem and found out that the nature of the issue can be corrected by performing pin alignment using the auto alignment feature of the prober. Enabling this feature will execute the pin alignment in every change of wafer (see Figure 10). The pin alignment consumed 15 seconds per wafer and had no major impact with the capacity since the hot testing set up for Resource 1 increased only with the average of 0.01%. This procedure was documented at PRC- 0002752 (Prober Wafer Parameter Settings).

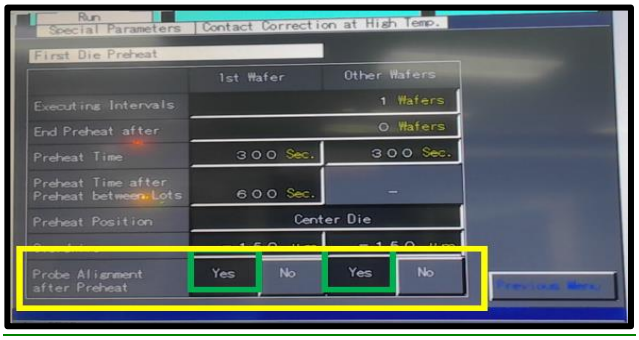

Figure 10. Enabling auto alignment feature of prober after Preheat on every change of wafer.

To apply across all HOT devices, the features as discussed above must be added to all device control maps. Control Maps are like a program that holds the wafer parameter settings of a certain device that the prober executes depending on what is defined – in this case, enabling the auto pin alignment. Currently we have a total of 67 control maps for HOT devices and after LEAN event, all control maps have been updated (see Figure 11).

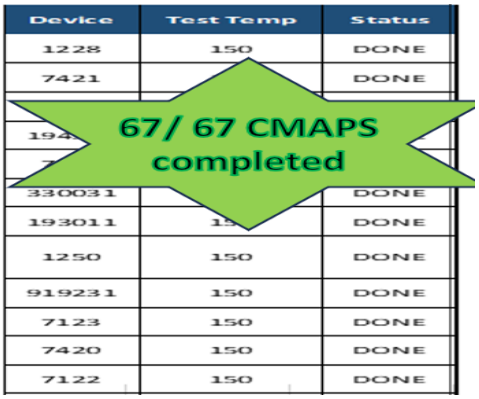

Figure 11. Fan out on of auto alignment feature on every change of wafer on other Hot testing devices.

3.2 Probe set up on Excessive Overdrive Setting

Overdrive is one of the important parameters that controls the pad penetration and or the contact of the pin to the pad. Specifically on Vendor A, a cantilever setup which produces a scrubbing motion during pin to pad contact. The higher the overdrive the larger scrub it will produce. It will induce probe damage once overdrive is set excessively. To prevent excessively high overdrive initial setting, all controls maps are adjusted by setting the overdrive value to Zero (0) with a maximum limit (see Figure 12).

The Special Instructions were created and documented in PRC- 0002752 (Prober Wafer Parameter Settings).

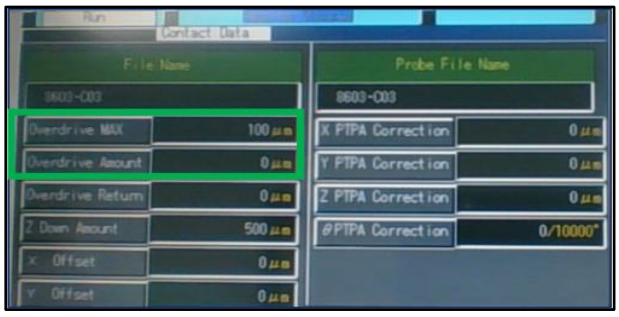

Figure 12. Overdrive setting default at 0 um (microns) and max limit (depending on vendor specifications).

3.3 Subjective acceptance call for probe mark alignment.

The team found out that the acceptance of probe marks is not at optimum location during device set up and qualification. All probe marks inside the bond pads including marks close to the border of the pads are being accepted (see Figure 13).

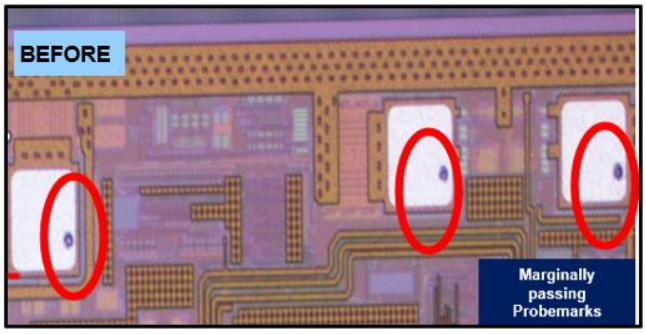

Figure 13. Subjective acceptance of probe marks near outside the boarder of the pad.

To reduce the wafer defects and correct the practice, the team created Probe marks Alignment templates for all devices based on actual bond pad size (see Figure 14). This template will be used by the operator as Go-No-Go reference for probe mark size and location. It was disseminated with the team and the procedure was updated in document WIN-0000645 (Operator Work Instruction) to include the use of probe mark template to check the probe mark alignment.

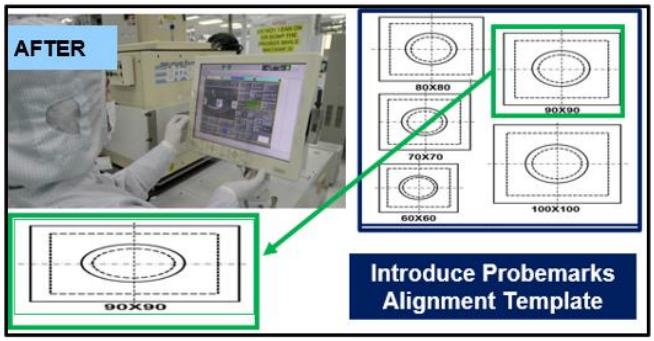

Figure 14. Probe marks alignment template.

3.4 No procedure to check epoxy during Probecard Maintenance (PM) and probe repair.

The hardware maintenance uses PM checklist during probe card maintenance and repair. All probe pins are checked and repaired. There is an event where the epoxy is already damaged and has crack that causes moving probe pins once

contacted to bond pads and this is not included in the checklist. The epoxy is a material that holds the probe pins to the ceramic post layer where the pins are inserted. As corrective actions, the team required to include checking of epoxy on all cards as part of maintenance and repair. Then, updated the document PRC-0002636 (AMPI Probe card Preventive Maintenance) (see Figure 15).

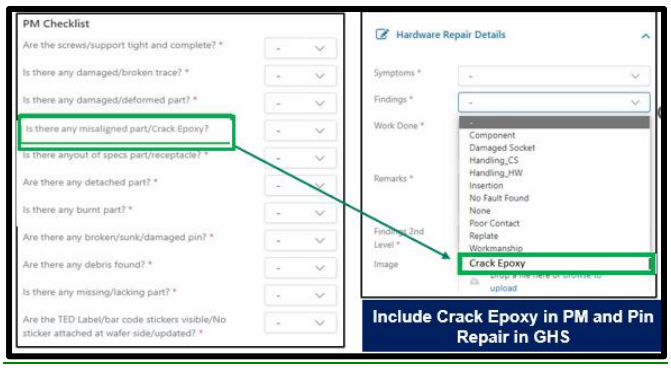

Figure 15. Crack Epoxy in Checklist from Global Hardware System (GHS).

3.5 Vibration coming from power generators.

In AMPI, testing of power generators is a regular activity as part of the Facilities maintenance. During these times, all machines located near the generator area experienced probe damage because of the floor vibrations affecting equipment stability. The probe mark locations are shifting to different locations about 16 microns in average (see Figure 16).

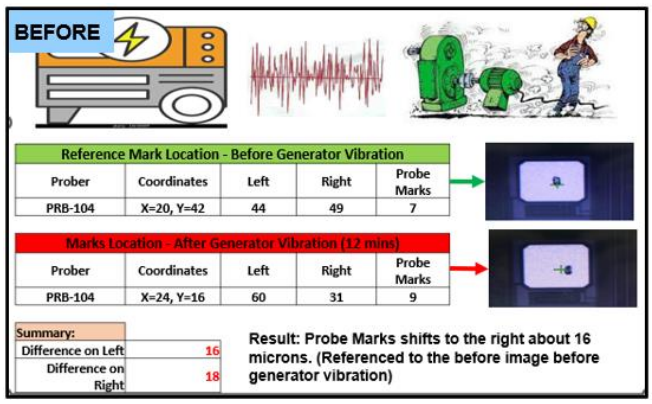

Figure 16. Reference Probe mark location

The team simulated an event and justified that generators testing is one of the factors that resulted in probe damage. As corrective action, the team created an OCP-0000059 (Probe Out of Control Action Plan) procedure - to STOP the machine during generator testing but only the machine nearest to the location or 5 meters to be exact. The probe pins or needle must be in CONTACT UP position or disengage to wafer. Then, resume testing once generator testing is completed (see Figure 17).

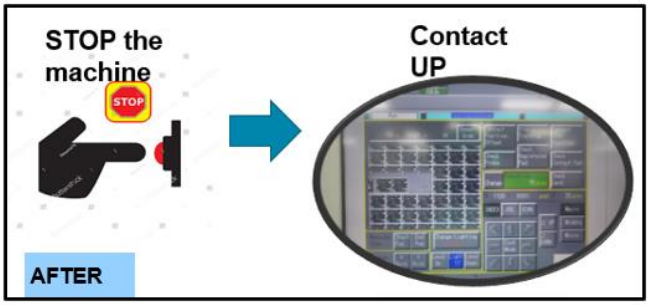

Figure 17. Out of Control Action Plan (OCAP) for testing of generators.

4.0 RESULTS AND DISCUSSION

The project aimed to reduce wafer defect probe damage by 50% or an average of 204 ppm for Resource 1. The baseline target is Q1-Q2 FY23 and Lean Workshop started on Q3FY23. After Lean ideas and improvement implemented on Q4FY23, from more than 300M die outs or processed qty there is a significant drop from 783 ppm to 122 ppm. Though it had an increase again on Q1FY24 to Q3FY24 but those are all not included in the targeted scope upon identifying the Lean Actions on Device 1 and Vendor A setups. For Q1FY24, the issue encountered was related to Machine or Camera problem while for Q2FY24, encountered Method issue as shifting marks at Cold process where the auto alignment improvement is not yet applied to Cold process and last for Q3FY24 encountered Method issue, which the defect induced from other facility and not yet applying the AMPI controls. All issues encountered are out of scope coverage. Then, it is notable that from January FY24, wafer defect probe damage significantly decreased to 43 ppm level and achieved the average of 117 ppm level or 71% improvement (see Figure 18).

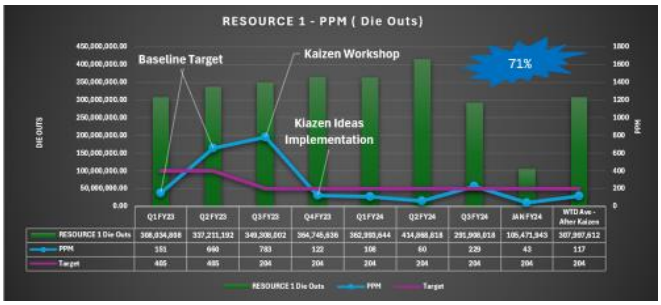

Figure 18. Wafer defect probe damage for Resource 1 (ppm level).

Moreover, the aim of this project is to reduce wafer defects for Device 1 which is the top device with the highest occurrences of wafer defect probe damage. The baseline data used is from Q1-Q2FY23, and the Lean activity started Q3FY23. Since Lean ideas and improvement implementation started last Q4FY23, wafer defect probe damage significantly reduced from 824 ppm to ZERO (0) ppm level or 100% improvement for Device 1 (see Figure 19).

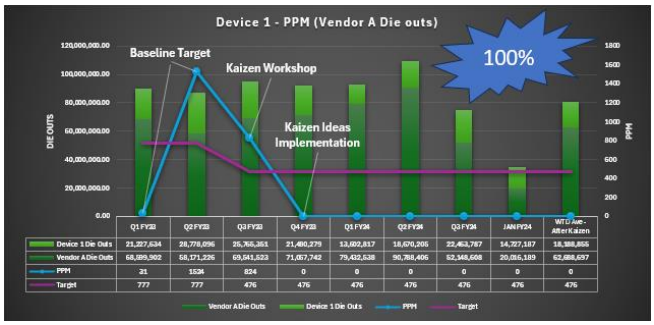

Figure 19. Wafer defect probe damage for Device 1 (ppm level).

The team performed significance testing (see Figure 20) in terms of yield via Minitab and the result of 0.1% yield improvement is significant. In terms of number of dice, 0.1% is equivalent to 135, 537 dice rejects. This resulted in cost avoidance of 174k PHP semiannual or 348k PHP per annum.

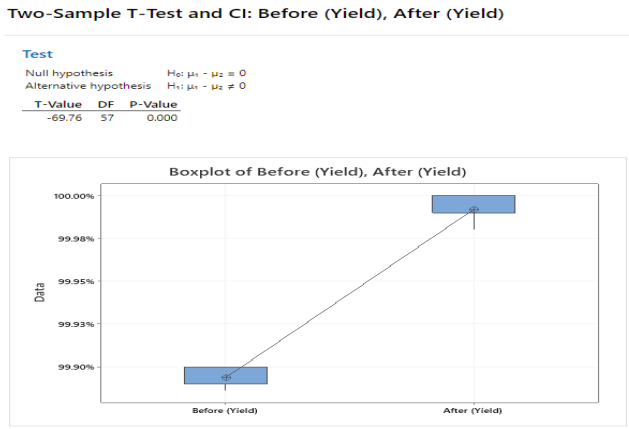

Figure 20. Two Sample T-Test of Before and After Yield shows significant yield improvement after implementation of corrective actions.

5.0 CONCLUSION

The top overall Probe Wafer Defect is probe damage which is primarily due to unoptimized pin alignment process of probe cards during every start of wafer probing. The team applied corrective action by enabling probe alignment after preheating on every change of wafers for HOT setup processes and it was proven as the main contributor of reduction of probe damage defect. In addition, the team discovered other effective improvement actions such as epoxy checking on probe cards, providing maximum Overdrive (OD) limit to avoid excessive overdrive setting, controls on vibration coming from generators, and by using of probe mark template as Go-No-Go reference for probe mark criteria acceptance.

Those actions mentioned above achieved the objective of reduction of probe damage wafer defects by 50% or an average of 338 ppm for all devices. Moreover, zero (0) defect was achieved specifically for Device 1 coming from 402 ppm or equivalent to 100% improvement after project implementation.

Moreover, the project reaped other metric performance deliverables such as cost avoidance, process enhancement, and cycle time improvements. Through the reduction of wafer probe damage defect, the team had avoided scrapping the die equivalent to 174k PHP or 348k PHP per annum for Device 1. Furthermore, it shortened the lead time through elimination queuing time for disposition and inspection process time of wafers affected with probe damage. The team was able to deliver our products with high yield, good quality and zero defects.

To ensure the sustainability of all the implemented projects, all procedures related to changes were all documented and updated in AMPI Probe Operation Work Instruction WIN-000645 (Operator Work Instruction), PRC-0002636 (AMPI Probe card Preventive Maintenance), PRC-0002752 (Prober Wafer Parameter Settings) and OCP-0000059 (Probe Out of Control Action Plan).

6.0 RECOMMENDATIONS

It is highly recommended to apply the LEAN tools and methodologies used in this project such as Gemba Walk (see Figure 21), Process Mapping (see Figure 22), Brainstorming (see Figure 23), root cause analysis by using Ishikawa or Fishbone diagram and performed Hypothesis testing to support further the identified problems are valid. By utilizing lean tools and techniques as framework in solving problems, it helped the team members to execute and implement appropriate corrective and preventive actions to deliver better results of achieving the target goal.

Figure 21. Practicing GEMBA Walk in probe production line seeing where the actual work happens.

Figure 22. Applying Process Mapping and identifying each process and marking detection and possible occurrences of the issue.

Figure 23. The team performs brainstorming, tackling, and discussing the issues and actions can be done.

The team also recommended all improvement actions to be applied on other Probe card types and to COLD Probe process set ups.

7.0 ACKNOWLEDGMENT

The authors would like to thank the following people for sharing their invaluable inputs for this study:

Their sponsor Probe Section Manager, Glenn Placido and Probe Department Manager, Maria Lourdes T. Balajadia; facilitator LEAN Section Manager Bernadette Palacio; and multi-disciplinary members, Lesley-Ann Padayhag, Melissa Grace Henera, Premian Rheycon, Christine Bartolome, John Edjelson Ramos, Ivy Balderama, Arlene Gallardo, Sheena Bongulan, Rodrigo Cruz, Joel Manuel, Nelson Murchante. Their contributions to the accomplishment of this study are highly appreciated.

8.0 REFERENCES

1. Figure 1 Image – https://www.seica.com/wafer-probe-card-test/

9.0 ABOUT THE AUTHORS

Victoria H. Acasio is a graduate of Bachelor of Science in Computer Science from the University of Batangas. She has 23 years of experience in the industry and is currently assigned as Section Head of Probe Production from Probe Department

Michael Angelo N. Carlos is a graduate of Bachelor of Science in Electronics and Communications Engineering from the Technological University of the Philippines Manila. He has 12 years of experience in the industry and is currently assigned as Senior Probe Engineering Supervisor from Probe Department

Milyn O. Embang is a graduate of Bachelor of Science in Electronics and Communications Engineering from the Saint Louis University Baguio City. She has 13 years of experience in the industry and is currently assigned as Senior Probe Process from Probe Department