LATCH-UP TESTER: HIDDEN THREATS BENEATH 100V/1A

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ABSTRACT

Characterizing latch-up robustness is necessary for all ADI parts before its release. This will help ensure that our products are compliant with industry standard JESD78. Doing this at the early stage of silicon development could help unfold potential weaknesses of the part which allows us to do revisions and meet customer expectations before market release. Any latch-up failure during the qualification run could delay the release of the parts, and any delay on breakthrough projects will probably cost not only dollars but also first-to-market opportunities. Even worse when those failures are due to hidden threats which are not detectable from the equipment itself.

Recent ESDA-Electrostatic Discharge Association paper entitled "Hidden Threats During Automated Latch-up Testing" tackle how these threats are resolved for 30V/5A supply. This paper will cover another voltage supply option and verify the resolution for 100V/1A. Latch-up evaluation for a current sense amplifier will serve as the use case to validate this claim.

1. 0 INTRODUCTION

ADI's quality mandate ensures that product releases will not be delayed. It is essential to address and resolve all probable failures before it could hold the market release of the part. Keeping our electrostatic discharge (ESD) test equipment upgraded and ESD folks updated on the latest trends could minimize the potential harm to our product releases. This way, we could guarantee that ADI will continuously be ahead of what's possible.

As part of the reliability requirement, devices require a latch-up (LU) test. A sanity check was done on sample units using the initial LU program developed two years ago. And during the pre-assessment activity, these units both passed the MK2 and automated test equipment (ATE). The program and test setup were then reserved for this assessment activity to ensure that there will be no discrepancy.

However, when the sample material arrived, it surprisingly had a 50% passing rate (3 out of 6 units) for 100mA while a 100% passing rate for a higher level of 150mA. This inconsistency called for revalidation by doubling the total number of units per level. Nonetheless, the failures persist – as we double the total population of stressed units, the number of failing units also doubled (6 out of 12 units).

To verify, both the program and results were forwarded to the product line for review. No issue was seen except for the sudden change in pre-current reading after the negative current injection when all inputs were held high.

Coincidentally, in the recently held ESDA Symposium 2022, a paper entitled "Hidden Threats During Automated LU Testing" discussed the same issue – failing at 100mA while passing at higher levels. The only difference is that they used a lower voltage supply of 30V/5A since their part only requires a low voltage. We are using the 100V/1A supply since the material has a maximum voltage of 70V.

That paper served as a reference in sanitizing and checking our own LU test equipment. We characterized both 30V/5A and 100V/1A supplies, and we also did an additional step of verifying the signal pin test (I-Test) based on JESD78, as shown in Table 1.

Table 1. Overview of latch-up tests for a complete latch-up characterization

Stress Type	Stress Polarity of Trigger	Input Pins Not Under Test (1)
Signal Pin Test (I-Test OR E-Test)	Positive current injection	Maximum pin operational voltage V_{maxOP}
		Minimum pin operational voltage V_{minOP}
	Negative current injection	Maximum pin operational voltage V_{maxOP}
		Minimum pin operational voltage V_{minOP}
Supply Test	Overvoltage	Maximum operational voltage V_{maxOP}
		Minimum operational voltage V_{minOP}

(1) All pins which are not excluded according to Section 5.4.1.

Actual verification proved the existence of overshoot and undershoot I-current at 30V/5A for all four conditions. For the 100V/1A supply option, undershoot I-current only occurred at the end of negative current injection where all inputs not under test were held high (VmaxOP) before transitioning to negative current injection where all input pins were held low (VminOP). The tester is only set to compare pre- and post-measurement with a delta of less than 10mA, and since the parameters are already shifted to a negative low because of the undershoot from the prior test, LU occurrence is not detected.

2. 0 REVIEW OF RELATED WORK

Refer to 1.0 Introduction.

3.0 METHODOLOGY

Unfolding the threat beneath the 100V/1A supply requires thorough evaluation. A series of designs of experiments (DOE) was created to reveal other potential threats that would likely occur from different JESD78 I-test conditions. All gathered data will be evaluated to know the current MK2 performance and to determine the necessary adjustment and eliminate these threats. Any modification will be confirmed and verified thru an actual material run. The team identifies a current sense amplifier as the assessment material for this set since this generic is sensitive to any current change.

Fig. 1 shows the actual Mk2 overshoot and undershoot process flow – from DOE to actual unit verification at post ATE. The authors would like to note that the actual DOE will only cover the standard JESD78 test condition for I-test particularly for existing ADI Mk2 equipment.

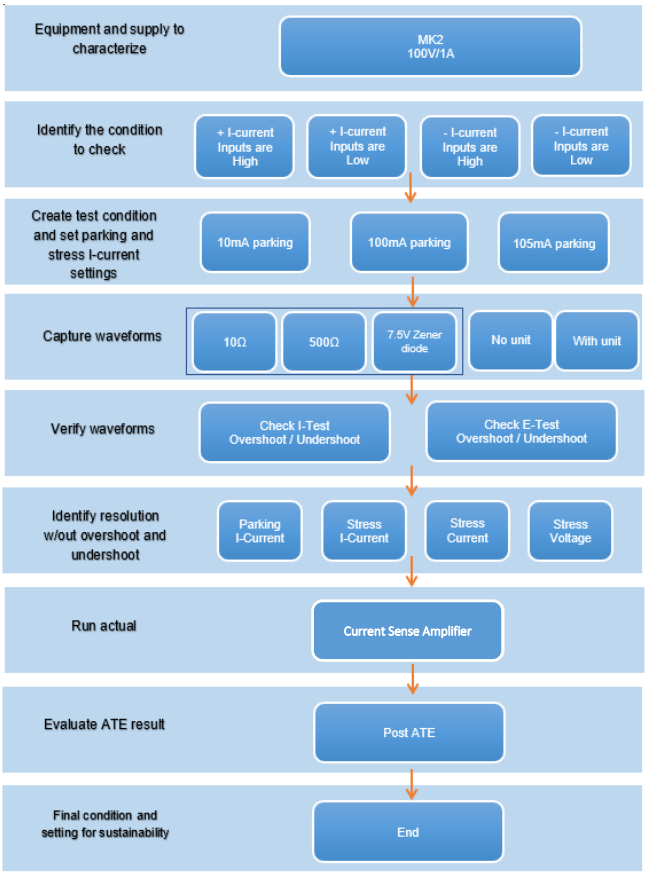


Fig. 1. High-level flowchart for the Mk2 hidden threat sanity check.

4.0 RESULTS AND DISCUSSION

To validate the occurrence of these threats, particularly for the ADI Mk2 equipment, the DOE settings in Table 2 were applied in testing the 30V/5A supply. Fig. 2 confirmed that overshoot and undershoot are indeed visible for all test conditions.

4.1. I-Test Overshoot Verification

Table 2. DOE Settings for 30V/5A Verification

	Parking I-current		parking voltage	clamp voltage	Stress I-current
DOE1	10mA	105mA	0V	5V	100mA
DOE2	10mA	105mA	0V	5V	-100mA
DOE3	-10mA	-105mA	5V	0V	100mA
DOE4	-10mA	-105mA	5V	0V	-100mA
DOE5	10mA	105mA	5V	0V	100mA
DOE6	10mA	105mA	5V	0V	-100mA

Fig. 2. 30V/5A waveform measurement for 10mA and 105mA parking.

Now that the threats are confirmed to be existing for 30V/5A, it is essential to validate the other supply option of 100V/1A. Table 3 shows the DOE for different voltage settings (Vsetting) – 5V, 30V, 35V, and 50V as shown in Figs. 3-6 respectively.

Table 3. DOE Settings for 100V/1A Verification

	Parking I-current			parking voltage	clamp voltage	Stress I-current
DOE1	10mA	100mA	105mA	0V	Vsetting	100mA
DOE2	10mA	100mA	105mA	0V	Vsetting	-100mA
DOE3	-10mA	-100mA	-105mA	Vsetting	0V	100mA
DOE4	-10mA	-100mA	-105mA	Vsetting	0V	-100mA
DOE5	10mA	100mA	105mA	Vsetting	0V	100mA
DOE6	10mA	100mA	105mA	Vsetting	0V	-100mA

Fig. 3. 100V/5A waveform for 5V setting.

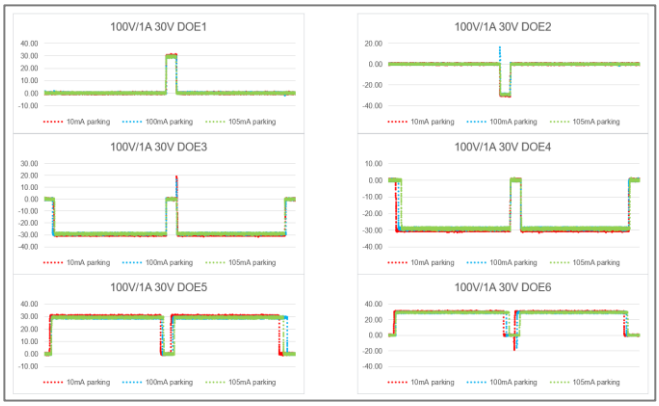


Fig. 4. 100V/5A waveform for 30V setting.

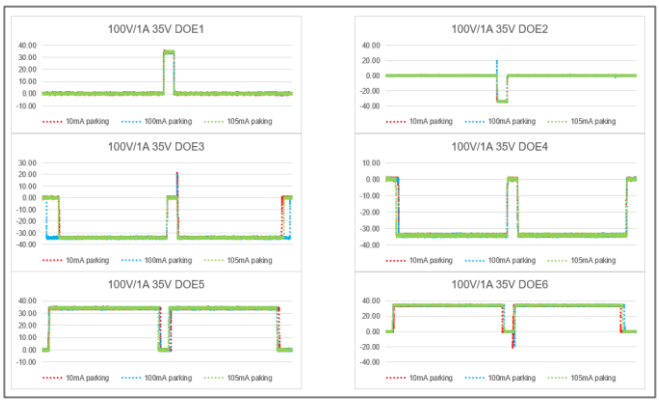


Fig. 5. 100V/5A waveform for 35V setting.

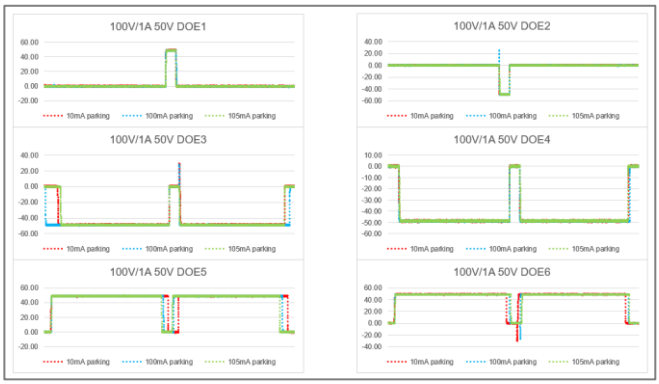


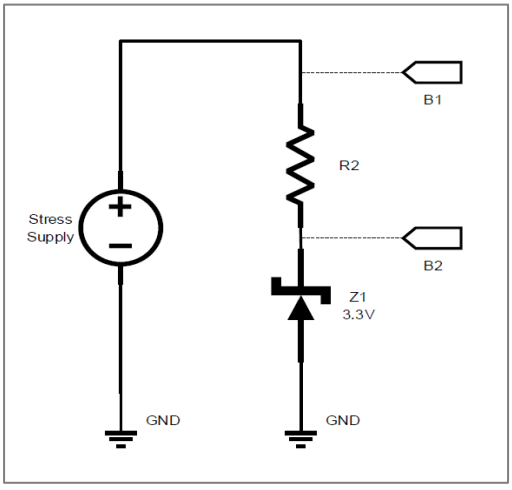
Fig. 6. 100V/5A waveform for 50V setting.

Table 4. Summary of I-Test V-voltage Overshoot

Voltage	Condition	100V/1A Parking I-current					
		10mA		100mA		105mA	
		OS	US	OS	US	OS	US
5V	DOE1	-	-0.6V	-	-	-	-
	DOE2	0.92V	-5.08V	2.07V	-7.51V	-	-
	DOE3	2.76V	-	2.08V	-7.46V	-	-
	DOE4	1.16V	-	0.64V	-	-	-
	DOE5	-	-1V	-	-0.64V	-	-
	DOE6	-	-2.58V	7.63V	-2.01V	-	-
30V	DOE1	-	-	-	-	-	-
	DOE2	-	-	16.8V	-	-	-
	DOE3	18.4V	-	16.5V	-	-	-
	DOE4	-	-	-	-	-	-
	DOE5	-	-	-	-	-	-
	DOE6	-	-18.4V	-	-16.7V	-	-
35V	DOE1	-	-	-	-	-	-
	DOE2	-	-	20V	-	-	-
	DOE3	22V	-	20V	-	-	-
	DOE4	-	-	-	-	-	-
	DOE5	-	-	-	-	-	-
	DOE6	-	-21.9V	-	-19.8V	-	-
50V	DOE1	-	-	-	-	-	-
	DOE2	-	-	28V	-	-	-
	DOE3	30.5V	-	28.5V	-	-	-
	DOE4	-	-	-	-	-	-
	DOE5	-	-	-	-	-	-
	DOE6	-	-30.8V	-	-28.6V	-	-

4.2. E-Test Overshoot Verification

Another stress type selection is E-test. However, this option would not always apply especially to low-impedance pins. Fig. 7 shows the actual test setup used to mimic the condition of low-impedance pins and to compute the total I-current overshoot. This setup shows how the overshoot behavior changes as the impedance gets higher – from 10 ohms to 100 ohms, and 500 ohms during E-test characterization.



. Fig. 7. I-current overshoot test setup

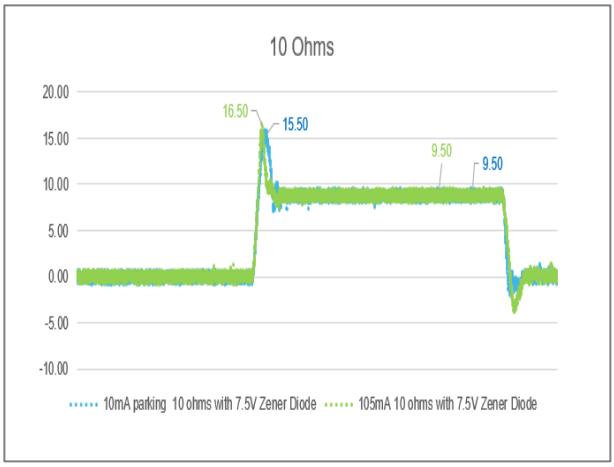


Fig. 8. Waveform at 10 ohms.

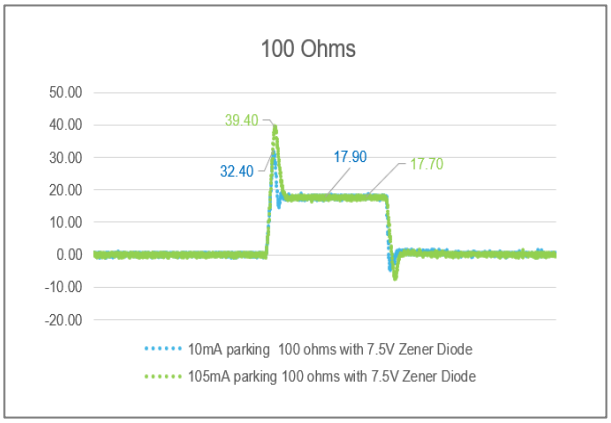


Fig. 9. Waveform at 100 ohms

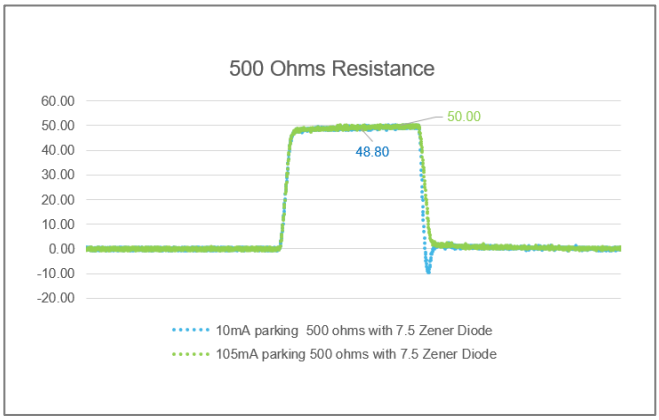


Fig. 10. Waveform at 500 ohms

To calculate the total over I-current induced during E-test for each pin impedance representation, we use the formula below:

$$\text{Over I-current(A)} = \frac{\text{Max Voltage(V)} - \text{High Voltage(V)}}{\text{Resistance}(\Omega)}$$

Table 5. Summary of E-Test I-current Overshoot

Resistance(Ohms)	Max(V)	High(V)	Overshoot (mA)
10	16.5	9.5	700
100	39.4	17.7	217
500	50	50	0

4.3. Actual Latch-up Testing

Both I-test and E-test configurations for the 100V/1A supply option displayed overshoot and undershoot I-current and V-voltage. To eliminate these surges, an optimized parking level of 105mA is essential during I-test as shown in Figs. 11-13 below. And when using E-test as a substitute, an impedance of 500 ohms and higher is required, as shown previously in Figs. 8-10.

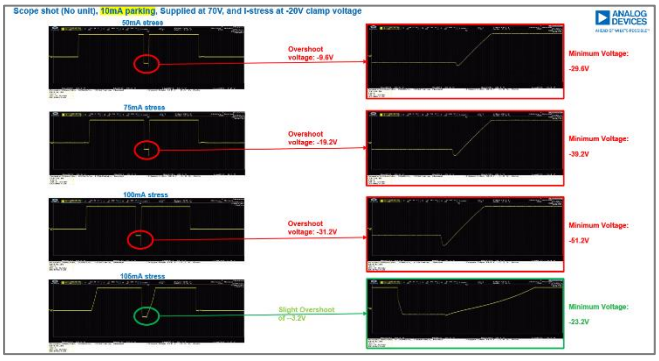


Fig. 11. Current Sense Amplifier LU testing at 10mA parking

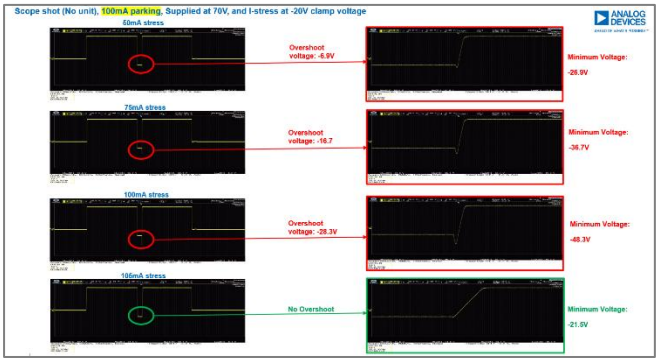


Fig. 12. Current Sense Amplifier LU testing at 100mA parking

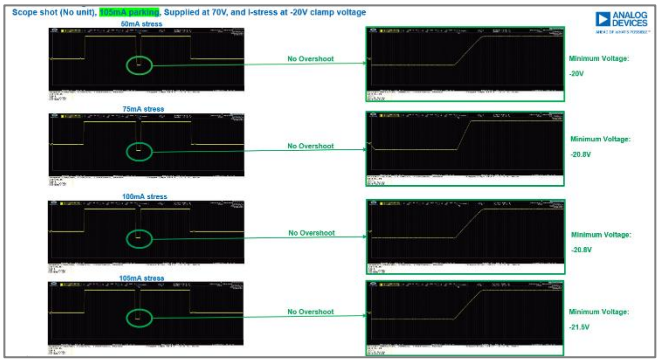


Fig. 13. Current Sense Amplifier LU testing at 105mA parking

4.4. ATE Test Results

Table 6. shows the actual sequence of event, and how we came up with 105mA parking level in resolving the previous post ATE failures. With this, we were able to meet the project assessment timeline.

Table 6. Summary of Post ATE Result

DATE	Condition	Device #	I-Test Level	MK2 Result	Post ATE	Final Result
2-Sep-22	Parking @ 10mA	1	100mA	Passed	Failed	Failed
		2		Passed	Passed	
		3		Passed	Passed	
		4		Passed	Failed	
		5		Passed	Passed	
		6		Passed	Passed	
		7	150mA	Passed	Passed	Passed
		8		Passed	Passed	
		9		Passed	Passed	
		10		Passed	Passed	
		11		Passed	Passed	
		12		Passed	Passed	
15-Sep-22	Parking @ 10mA (revalidation)	1	100mA	Passed	Passed	Failed
		2		Passed	Passed	
		3		Passed	Failed	
		4		Passed	Passed	
		5		Passed	Failed	
		6		Passed	Failed	
		7		Passed	Failed	
		8		Passed	Failed	
		9		Passed	Passed	
		10		Passed	Passed	
		11		Passed	Passed	
		12		Passed	Failed	
13-Oct-22	Parking @ 105mA	1	100mA	Passed	Passed	Passed
		2		Passed	Passed	
		3		Passed	Passed	
		4		Passed	Passed	
		5		Passed	Passed	
		6		Passed	Passed	
		7		Passed	Passed	
		8		Passed	Passed	
		9		Passed	Passed	
		10		Passed	Passed	
		11		Passed	Passed	
		12		Passed	Passed	

5.0 CONCLUSION

For ADI Mk2 equipment, the overshoot and undershoot are evident in all conditions at 30V/5A supply. While for 100V/1A supply, the undershoot current only appears when parking I-current and stress I-current has different polarity.

The rest of the conditions do not show any overshoot or undershoot even when it is parked at our usual 10mA.

Trigger pulse overshoots and undershoots can be avoided by limiting the signal pin stress by doing either of the following steps:

- Ensure pin impedance of higher than 500 ohms for E-test.
- Stressing at a higher parking range of 105mA for I-test. This slight 5mA increase from the usual stress current of 100mA is confirmed to be not harmful to the part as this is merely a starting point to enable the 1A supply and eliminate the overshoot, all based on the post-ATE results.

This development in our process would be beneficial should there be upgrades in the software, or if we would experience serious breakdowns in the future. The paper would also serve as a guideline for verifying and qualifying alternative equipment for ESD and LU tests.

6.0 RECOMMENDATIONS

Refer to 5.0 Conclusion.

7.0 ACKNOWLEDGMENT

Special thanks to Raymond Sietereales, Stephen Heffernan, Quan Wan, Ke Chen, Jaylord Bautista for helping us verify our DOEs.

8.0 REFERENCES

1. Scott Ward, Marty Johnson, Michael Stockinger, Sheela Verwoerd, Tom Meuse, Greg O'Sullivan, Robert Ashton, Jordan Dye, **Hidden Threats During Automated Latch-up Testing**

2. ESDA, **JESD78E**

9.0 ABOUT THE AUTHORS

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10.0 APPENDIX