HIGH-PRECISION SELECTIVE BACKSIDE DECAPSULATION TECHNIQUE FOR EFFECTIVE FAULT SITE IDENTIFICATION OF DUAL-DIE DEVICE DIE-LEVEL FAILURES

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ABSTRACT

Semiconductor devices have become increasingly complex in functionality and package structure. Several devices with advanced package construction have dual or multiple die (either stacked or side by side) in a single package. This advancement in packaging technology presents a challenge to failure analysis during the decapsulation process and fault isolation analysis. It is anticipated that an incident with functional failure that is categorically under a high complexity factor requires careful in-depth analysis since it is typically just a single unit. The device must be electrically testable and still functional after the decapsulation process. Based on the 3-month data of the completed failure analysis (FA) this year alone, 35% of higher complexity factor submitted units either had packages that incorporated multiple die, assembled with wire downbond and fragile glass lid designs (such as image sensors devices).

These types of package structure configurations require a high-precision decapsulation process to ensure the electrical integrity of the device for fault isolation analysis.

This paper presents a case study of one of the customer-returned incidents involving a device with both dual-die and wire downbound package configurations. A functional test-related failure was successfully analyzed, and the cause was identified using an internally developed technique regarding high-precision selective backside decapsulation process.

Keywords — Functional failure, Failure Analysis (FA), Selective Backside Decapsulation, Laser Ablation, Wet Etch, X-prep Precision Milling, Flag or Paddle

1. 0 INTRODUCTION

Looking at the 3-month data from 2024 completed failure analysis (FA) reports, 35% of the higher complexity factor submitted units had packages that had multiple die, were assembled with wire downbond, and some had fragile glass lid designs such as image sensor devices (Figure 1). The majority of these devices are also automotive devices.

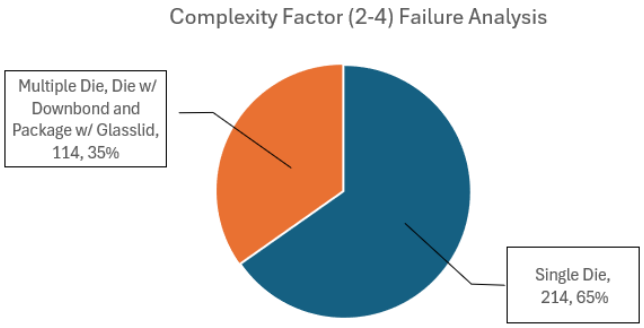

Fig. 1. Jan-Mar 2024 FA Completed Reports. This graph shows that 35% (114) of the higher complexity factor submitted units are either Multiple Die or Die with Downbond or Package with Glasslid.

Among these automotive devices are High Voltage Isolated Drivers for low-end cost and board space-sensitive applications. See Figure 2.

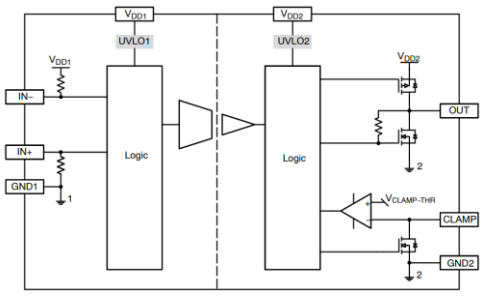

Fig. 2. Device Simplified Block Diagram. This provides the device's simplified operation and major parts.

The device serves as a high-current gate driver for single-channel IGBTs and MOSFETs. It accepts complementary inputs and, based on the pin configuration, provides separate high and low driver outputs (OUTH and OUTL) for ease of system design. Additionally, the driver is compatible with input bias voltages and signal levels ranging from 3.3 V to 20 V.

The device has a dual-die configuration and is available in a narrow-body SOIC-8 package. It also has a dual flag or paddle with a wire down-bond that connects the GND pins. See Figure 3.

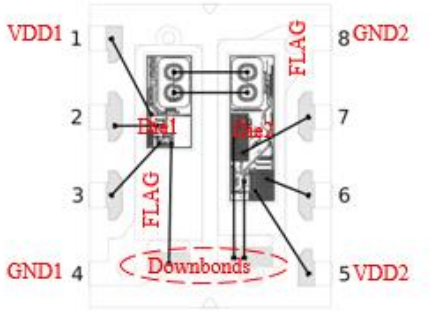

Fig. 3. Device Drawing. This shows the Narrow-body SOIC-8 package device structure with dual flag or paddle with wire downbond.

The device die layout review disclosed six (6) metal layers and a top metal blanket design (Figure 4) that can obscure the emission sites from being detected at the die surface if topside decapsulation is performed.

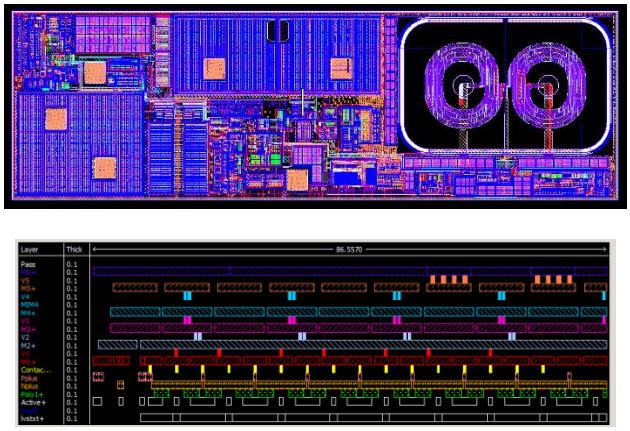

Fig. 4. Device Die2 Layout and Cross-section. It shows the physical design and internal structure of the device.

Based on brainstorming with the failure analysis (FA) team, the selective backside decapsulation approach was decided as the appropriate method to proceed with the destructive analysis. With this technique, only the problematic die in this case (Die2) will be exposed for fault isolation analysis. The challenge here was that the flag or paddle is connected to the ground pin and that connection must be preserved to ensure that the device's electrical integrity and still functional during the course of the analysis. In addition, after selective backside decapsulation was done, the unit must still allow and be suitable for die topside decapsulation in case in-circuit probing is necessary.

There are four (4) different techniques for package backside decapsulation. These are Backside Mechanical Polishing / Grinding, Chemical Etching, Manual Mechanical decapsulation, and finally, Mechanical Milling using a precision milling tool.

A comparative analysis was performed on different backside sample preparation techniques. It aims to identify the most effective method when selective backside decapsulation on multiple die is required (Table 1).

Table 1. Comparative Analysis of different Backside Sample Preparation Process when dealing with Multiple Die with Downbonds

Techniques	Accuracy / Consistency (20%)	Backside Die Inspection using IR (20%)	Testability / Preserve Electrical Functionality (25%)	Can Perform Several Fault Isolation Technique i.e OBIRCH, PEM & In-circuit Probing (25%)	Process Time (10%)	Scoring Total
1. Backside Mechanical Polishing/Grinding	1	1	0	0.5	0	52.50%
2. Chemical Etching	0.5	1	0.5	0.5	1	65%
3. Manual Mechanical Decapsulation	0	1	0.5	0.5	0.5	50%
4. Mechanical Milling using Precision Milling Tool (X-Prep)	1	1	1	1	0.5	95%
Scoring Criteria	Description					
1	Process is achievable and can be successfully completed.					
0.5	Process might be achieved but not consistently successful.					
0	Unit damaged / No chance of recovery / Process not acheivable					

Based on the comparative analysis table, two of the techniques have high total scoring results.

95% - Mechanical Milling using Precision Milling Tool
65% - Chemical Etching

Experiments were conducted to further identify the most effective backside decapsulation method on multiple die devices with downbonds and suitable to preserve the device's electrical integrity during the analysis.

2. 0 REVIEW OF RELATED WORK

Refer to 1.0 Introduction.

3.0 METHODOLOGY

Discussed in this section are the experiments performed in the study to compare the effectivity of the selected Backside Sample Preparation Processes when dealing with multiple die with downbonds.

The decapsulation process involves removing the mold compound from the surface of a semiconductor die. By doing so, the internal features of the die become visible, enabling inspection for any anomalies. This step serves as preparation for subsequent fault isolation techniques.

3. 1 EXPERIMENT 1

Performed selective backside decapsulation using a laser ablation tool to remove a portion of the mold compound, then wet etch to etch out the flag.

1st step: Exposed the flag of the problematic die (Die 2) using the laser ablation tool. A portion of the mold compound will be removed to expose the flag of Die 2 (Figure 5).

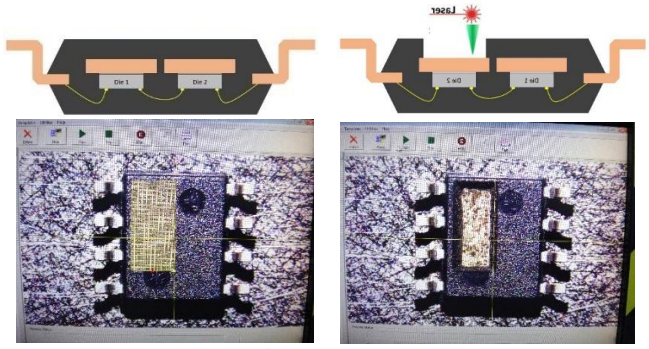

Fig. 5. Laser ablation results of Experiment 1. These images shows the successful laser ablation results in exposing the Die 2 flag.

2nd step: Wet etching was performed using a 70% Nitric acid concentration to etch out portions of the Die 2 flag and expose the die backside (Figure 6).

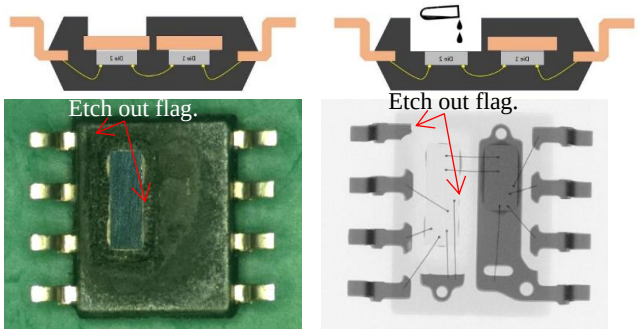

Fig. 6. Wet etching and X-ray analysis results. X-ray image shows that most of the flag were etched out.

Die 2 was successfully exposed. However, the x-ray image showed that it failed to retain a portion of the flag.

Experiment 1 summarized results are shown in Table 2.

Table 2. Experiment 1 Decapsulation Method Results

Backside Decapsulation	Mold Compound Removal	Result	FLAG Removal	Result
Experiment 1	Laser Ablation	✓	Wet Etch (70% Nitric Acid)	X

Wet etching FAILED to retain some portion of the flag that is necessary for the GND connection.

3. 2 EXPERIMENT 2

Performed selective backside decapsulation using a laser ablation tool to remove a portion of the mold compound, then precision milling to remove the flag.

1st step: Exposed the flag of Die 1 and Die 2 using the laser ablation tool. A portion of the mold compound will be removed to expose the flag (Figure 7).

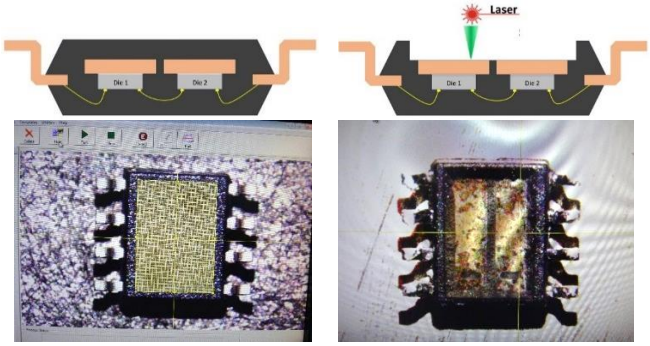

Fig. 7. Laser ablation results of Experiment 2. These images shows the successful laser ablation result in exposing the Die 1 and Die 2 flag.

2nd step: Precision milling was performed on the portion of the Die 2 flag to expose the die backside (Figure 8).

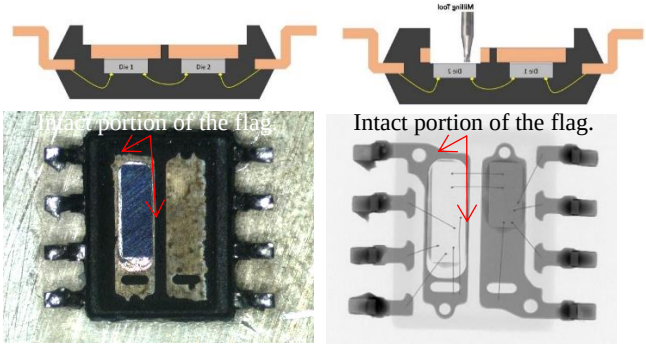

Fig. 8. Precision milling and X-ray analysis results. X-ray image shows that after precision milling a portion of the flag was retained.

Die 2 was successfully exposed. The x-ray image showed a retained portion of the flag.

Experiment 2 summarized results are shown in Table 3.

Table 3. Experiment 2 Decapsulation Method Results

Backside Decapsulation	Mold Compound Removal	Result	FLAG Removal	Result
Experiment 2	Laser Ablation	✓	X-prep Precision Milling	✓

Precision milling SUCCESSFULLY retains some portion of the flag that is necessary for the GND connection.

4.0 RESULTS AND DISCUSSION

Successful high-precision selective backside decapsulation and topside decapsulation were done on the identified device (Figure 9).

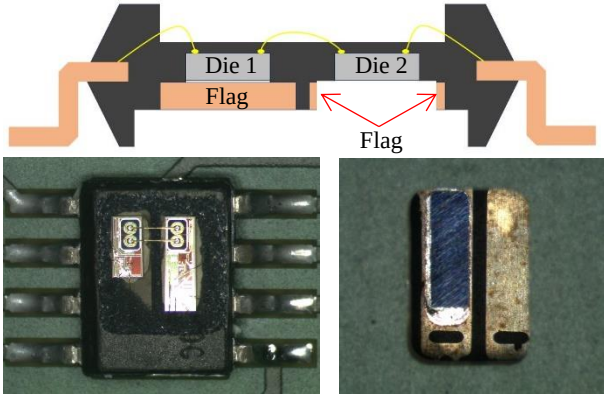

Fig. 9. Topside and high precision backside decapsulation results. The images show the successful topside decapsulation and high-precision selective backside decapsulation with intact portion of the flag (GND connection).

High-precision selective backside decapsulation process for this device was divided into two sub-processes. Laser ablation and precision milling processes.

Laser Ablation refers to the technique of utilizing a regulated laser beam to extract material from a solid substance. This method is versatile and can be employed on a wide range of materials, including but not limited to metals, semiconductors, glass, ceramics, polymers, wood, stone, and various biological materials, with the use of numerous types of lasers [2].

Laser ablation basic parameters for removal of Gxxx mold compound:

- Laser Current: 50.00
- LaserQSwitch: 40.00
- DutyCycle: 1
- Speed: 500.00
- Passes: 1

Laser ablation was done by hastening the exposure of the area to be removed and running the laser ablation tool following the basic parameters. This completes the initial step in sample preparation.

The next step incorporates the X-PREP Precision Milling, it is a specialized 5-axis CNC-based milling/grinding/polishing machine designed to support electrical and physical failure analysis techniques and other applications requiring high-precision sample preparation [3].

X-Prep precision milling set-up parameters (Figure 10).

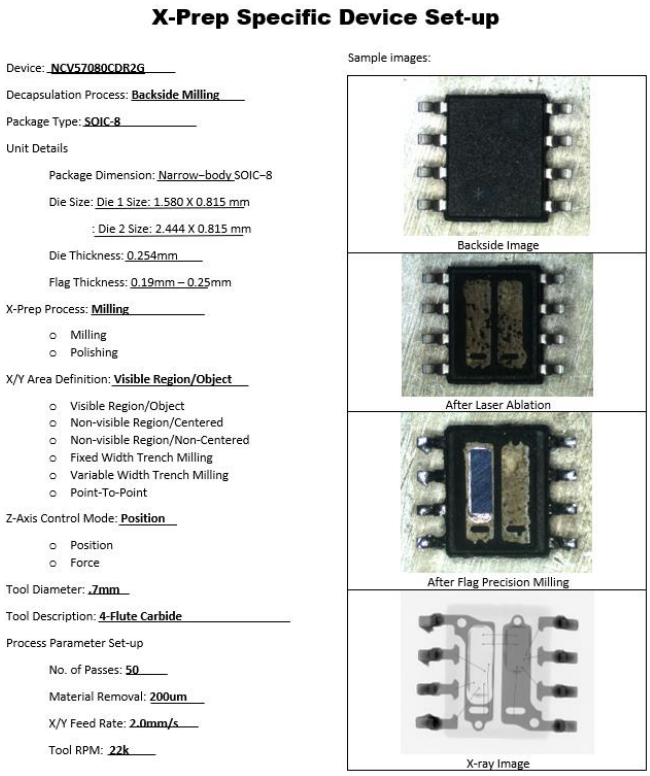

Fig. 10. X-Prep Milling Specific Device Set-up. This shows the precision milling set-up parameters.

Precision milling requires a specific set-up for every device family, depending on the device package structures. It uses a combination of proper drill bit , speed and area definition for proper sample preparation.

High-precision selective backside decapsulation process was successfully done to the returned unit. It effectively preserves the flag electrical connection and ensures the device's functionality during the analysis of the below case study.

Case Study: Functional failure (IDD2 failure)

4.1 Failure Characterization

The customer's problem statement reads, in part: "Failed driver during an end-of-line verification."

The returned units were confirmed to have failed on the Automated Test Equipment (ATE) retest (Figure 11) and the functional bench test validation using the IDD2 test (Figure 12). However, no curve trace abnormalities on all pins were observed (Figure 13).

Excerpt of ATE retest results confirmed the IDD2 test failure.

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CRU1
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 3.10   0.634   MA   0.000   2.000    IDD1-0-3p3, VD1=3.3V, VD2=15V, IN+=0V, IN-=0V
 3.11   0.671   MA   0.000   2.000    IDD1-0-5, VD1=5.0V, VD2=15V, IN+=0V, IN-=0V
 3.12   0.774   MA   0.000   2.000    IDD1-0-15, VD1=15V, VD2=15V, IN+=0V, IN-=0V
 3.19   4.381   MA   0.000   5.500    IDD1-100-5, VD1=5.0V, VD2=15V, IN+=VD1, IN-=0V
 3.30 102.036   MA   0.000   2.000 FAIL IDD2-0-15, VD1=5.0V, VD2=15V, IN+=0V, IN-=0V
 3.38 102.036   MA   0.000   2.000 FAIL IDD2-100-15, VD1=5.0V, VD2=15V, IN+VD1, IN-=0V

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CRU2
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 3.10   0.628   MA   0.000   2.000    IDD1-0-3p3, VD1=3.3V, VD2=15V, IN+=0V, IN-=0V
 3.11   0.671   MA   0.000   2.000    IDD1-0-5, VD1=5.0V, VD2=15V, IN+=0V, IN-=0V
 3.12   0.774   MA   0.000   2.000    IDD1-0-15, VD1=15V, VD2=15V, IN+=0V, IN-=0V
 3.19   4.619   MA   0.000   5.500    IDD1-100-5, VD1=5.0V, VD2=15V, IN+=VD1, IN-=0V
 3.30 102.036   MA   0.000   2.000 FAIL IDD2-0-15, VD1=5.0V, VD2=15V, IN+=0V, IN-=0V
 3.38 102.036   MA   0.000   2.000 FAIL IDD2-100-15, VD1=5.0V, VD2=15V, IN+VD1, IN-=0V
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Fig. 11. ATE retest results. This shows the functionality test response of the device.

Scope plot of IDD2 bench test results. Returned units were confirmed to have failed on IDD2 test.

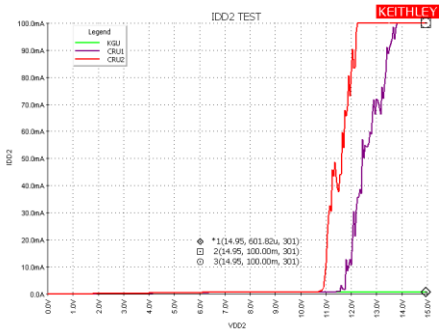


Fig. 12. IDD2 bench test results. A Bench test plot showing the device response to the specific test parameters.

Snapshot of curve trace validation results. No curve trace abnormalities on all pins were detected.

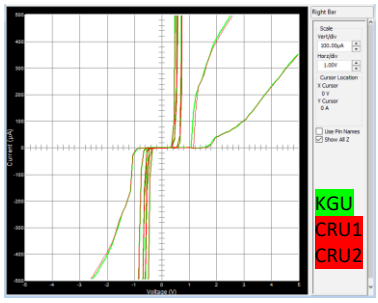


Fig. 13. Curve trace validation results. This plot shows the pin-to-pin curve trace conducted by shorting all pins to ground and then sweeping the pin under test.

The units were confirmed to have valid electrical failures and will proceed with further failure analysis flow, which includes non-destructive and destructive analysis.

4.2 Non-destructive Analysis

Non-destructive analysis such as X-ray microscopy analysis (Figure 14) and Scanning Acoustic Tomography (SAT) analysis (Figure 15) to inspect package internal parts.

X-ray image of unit, top and side view. No problems were found.

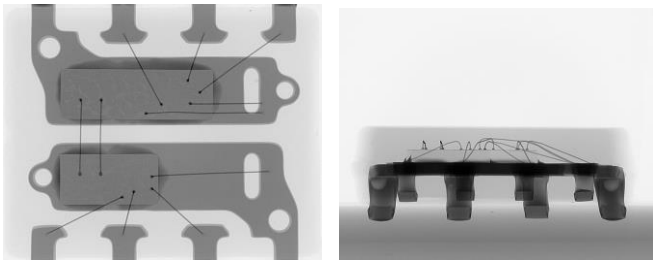


Fig. 14. X-ray analysis results. X-ray images show a detailed view of the internal structure of the device.

Scanning Acoustic Tomography (SAT) image. No package delamination was detected.

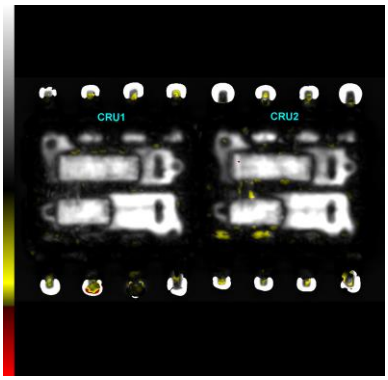


Fig. 15. Scanning Acoustic Tomography (SAT) analysis results. It detects delamination by using acoustic microimaging.

Non-destructive analysis results showed no package-related problems were found on the returned unit.

4.3 Destructive Analysis

Destructive analysis such as decapsulation (Figure 16), microscopic inspection, and electrical fault isolation (EFI) (Figures 17 - 20) were performed to identify the root cause of the problem. The decapsulation process was one of the most critical and difficult, especially for function failures. The returned unit must still be functional and testable after the decapsulation process. Then, electrical fault isolation (EFI), such as Optical Beam Induced Resistance Change (OBIRCH) and Photoemission Microscopy (PEM) will be performed.

4.3.1 Decapsulation

A topside and high-precision selective backside decapsulation process was successfully done on the returned unit. The device package, die, and bond wire's microscopic inspection showed no damages or defects (Figure 16).

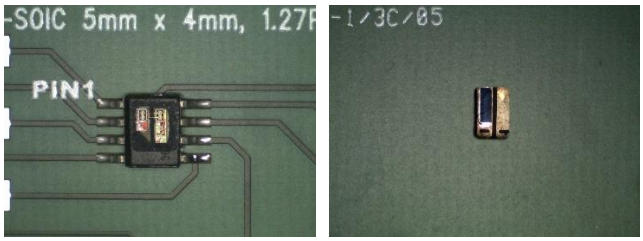
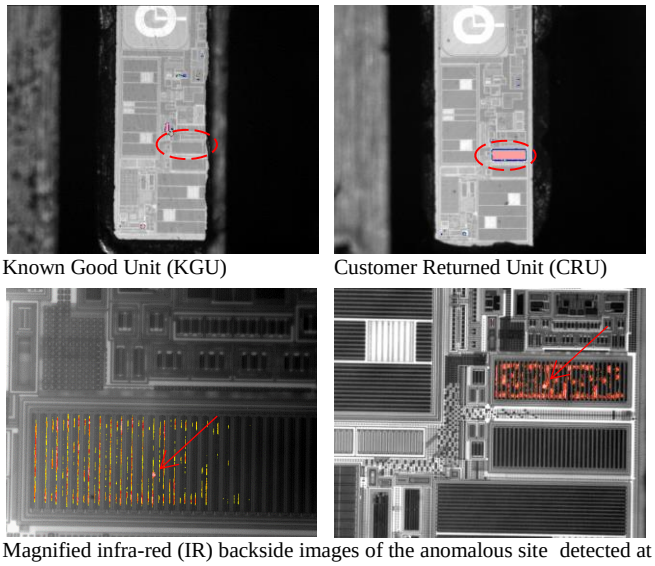


Fig. 16. Topside and High-precision selective backside decapsulation results. The images show the successful topside decapsulation and high-precision selective backside decapsulation with intact portion of the flag (GND connection).

4.3.2 Electrical Fault Isolation (EFI)

Electrical fault isolation (EFI) was done using Photoemission Microscopy (PEM) analysis biased on the device's failing state (Figure 17). An anomalous emission site was detected at the returned unit, indicating a potential cause of failure.



Known Good Unit (KGU) Customer Returned Unit (CRU)

Magnified infra-red (IR) backside images of the anomalous site detected at the returned unit.

Fig. 17. Photo emission (PEM) backside image of die during fault isolation. This shows that an anomalous emission site was detected at the CRU.

Topside Photoemission Microscopy (PEM) analysis was also conducted which showed no significant emission sites (Figure 18).

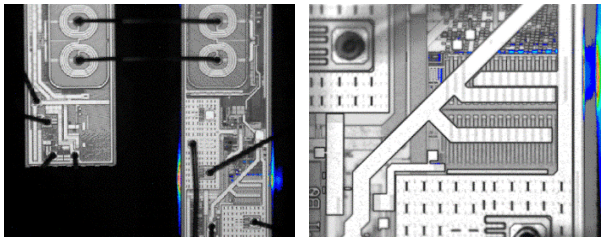


Fig. 18. PEM die topside image of die during fault isolation. This shows that there is no significant anomalous emission sites detected on the CRU.

Layout and schematic review traced the anomalous point emission site within the MLD1 transistor of the ESD_Top protection circuitry (Figure 19).

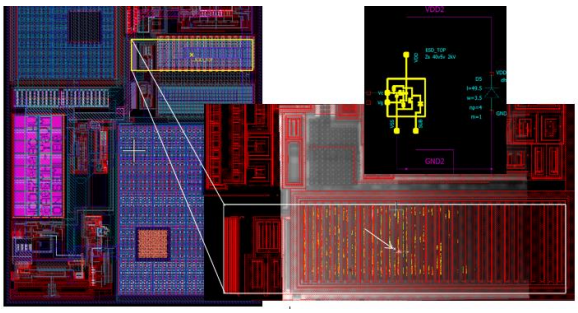


Fig. 19. Partial layout and schematic of the device. The Layout and schematic review shows that the anomalous point emission site was within the MLD1 transistor of the ESD_Top protection circuitry.

A Progressive Focused Ion Beam (FIB) cross-section was then conducted focusing on the anomalous PEM spot to further visualize the defect site. The results disclosed an anomalous bridging on the silicon substrate to the polysilicon gate of the MLD1 transistor (Figure 20).

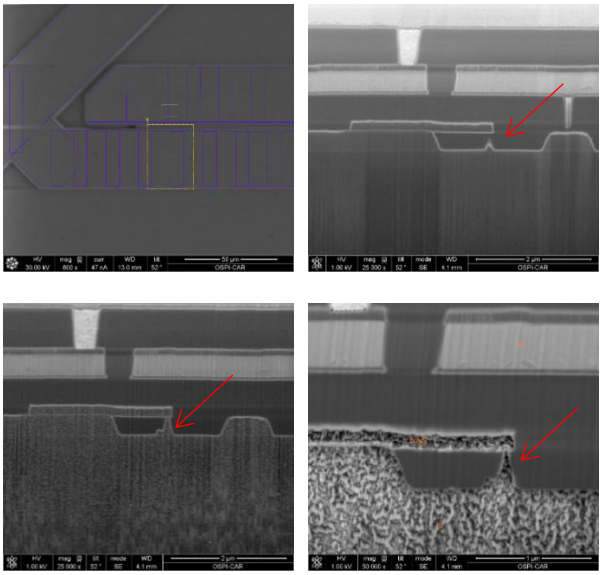


Fig. 20. Progressive FIB cross-section results. The result shows that the identified anomalous spot disclosed an anomalous bridging of the silicon substrate to the polysilicon.

The customer's reported failure was confirmed on the returned unit. The device failed due to a faulty MLD1 transistor component caused by anomalous bridging between the silicon substrate and the polysilicon.

Precision milling was utilized throughout the decapsulation process of the majority of the 35% higher complexity factor submitted units with advanced package structures. Precision milling was used on selective backside decapsulation, glass lid removal for image sensors, and die substrate thinning for highly doped devices.

5.0 CONCLUSION

Based on the results gathered from this study, the high-precision backside decapsulation process technique was proven to be an effective method for destructive analysis on multiple die devices with downbonds. It is a highly suitable method to preserve the device's electrical integrity during the analysis. In addition, after the backside decapsulation process, the device was still intact and suitable for topside decapsulation if in-circuit probing was necessary.

6.0 RECOMMENDATIONS

Because of the importance of preserving the device functionality on the returned unit, it is recommended that the decapsulation process be performed first on a known good unit before proceeding to the customer-returned unit. The process can be used to guide the decapsulation of other advanced package devices such as multiple die, w/ down-bond, and device packages with glass lids, such as image sensors. However, a device-specific setup for decapsulation is recommended.

7.0 ACKNOWLEDGMENT

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9.0 ABOUT THE AUTHORS

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