# Effective Failure Analysis Approach in Uncovering Gate-to-Drain/Source Tungsten Spur Fabrication Defect

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## *ABSTRACT*

The accurate determination of the failure mechanism is a foundational step in quality control, process improvement, and business success, significantly impacting customer satisfaction. The comprehensive failure analysis revealed a Gate-to-Drain/Source (D/S) Tungsten (W) spur defect.

Identifying the defect was a challenge that demanded advanced techniques to successfully determine the exact failure mechanism. It requires schematics and layout review through Avalon, Light Emission Microscopy (LEM) and Optical Beam Induced Resistance Change (OBIRCh) analysis to localize the failing circuitry, Passive Voltage Contrast to localize the failing transistor and Nanoprobing coupled with Electron Beam Induced Resistance Change (EBIRCh) technique to localize the leakage location between the transistor's Gate-to-D/S region. Focused Ion Beam (FIB) cross section was the preferred physical failure analysis approach rather than top down chemical deprocessing as the latter technique etched away the tungsten spur. Furthermore, the defect site in a chemically deprocessed unit maybe misinterpreted as an Electrically Induced Physical Damage given the silicon pits' semblance to the appearance of an Electrostatic Discharge (ESD) damage. Elemental analysis post FIB cross sections and Transmission Electron Microscope (TEM) confirmed the elemental composition of the defect to be Tungsten.

Investigation results from the fabrication site revealed that the defect occurred due to a breach of the Titanium Nitride (TiN) barrier at the bottom of the poly contact. The breach can occur in rare circumstances when the contact intersects with the spacer nitride. Critical dimension (CD) tightening was implemented at the fabrication site to address the defect.

## 1.0 INTRODUCTION

This paper presents the effective failure analysis process and utilization of advanced FA techniques that led to the identification of the failure mechanism involving a fabrication defect on a Hot Swap Controller and Digital Power Monitor parts which was assembled into a 48-lead Lead Frame Chip Scale Package (LFCSP). Furthermore, it explores the novel challenges encountered with these techniques, provides insights into overcoming them and enhancing the effectiveness moving forward.

## 2.0 REVIEW OF RELATED WORK

### *2.1 Failure Analysis of Tungsten Stud Defects from the CMP Process*

Research in semiconductor manufacturing demonstrating the effectiveness of combining multiple analytical techniques to isolate and identify a tungsten stud defect. The authors utilized methods such as SEM, TEM, and FEAES with FIB preparation to pinpoint the defect.[1]

### *2.2 Failure Analysis of Tungsten Contact Failure in a 0.13 µm CMOS Process*

A reference study where electrical shorts were observed between tungsten contacts, necessitating comprehensive failure analysis methodologies that combine electrical and physical testing approaches.[2]

## 3.0 METHODOLOGY

### *3.1 Recommended Approach*

Advanced techniques were utilized to overcome precision limitations and enhance the efficacy of failure analysis processes. The cognitive approach to analyze the functionality issues can be seen on the process flow on Fig. 1.

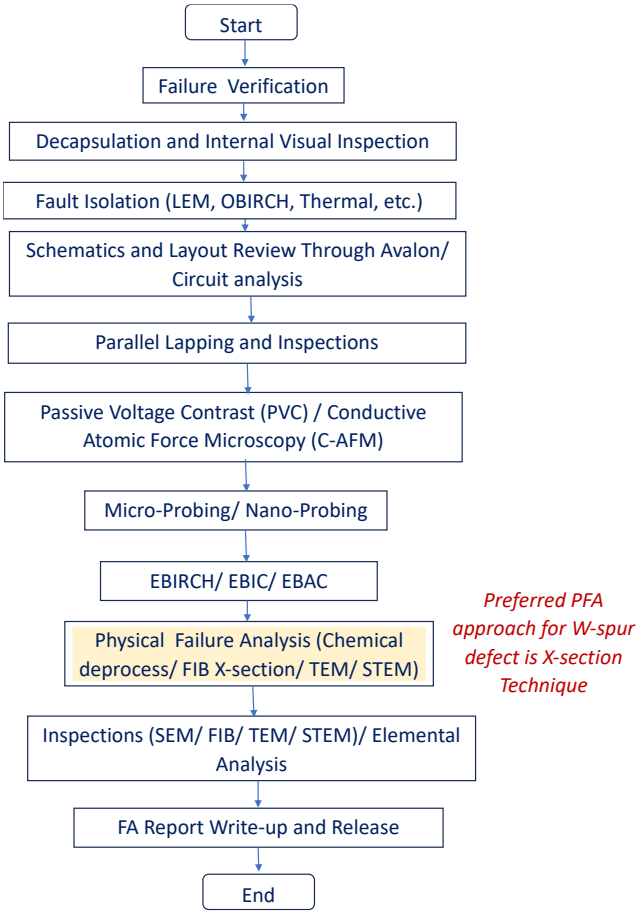



Fig. 1. The failure analysis process

## *3.2 Key Failure Analysis Techniques in the Identification of the Fabrication Defect*

### *3.2.1. Passive Voltage Contrast*

Passive Voltage Contrast (PVC) method using Scanning Electron Microscope (SEM) or Focused Ion Beam (FIB) for failure localization allows non-contact identification of open, resistive and leaky circuits is a widely accepted fault isolation technique in semiconductor FA community. The interaction of a charged particle beam with structures of different electric conductivity in a microelectronic circuit locally changes the electric potential at its surface. When electron beam strikes the surface a conductor, it depletes the negative charge from the target unless the target is grounded. Therefore, a floating conductor will tend to charge positive and appear darker in the secondary image than similar grounded structure. With the same reason, the secondary image of reverse biased contact will be darker than that of a forward biased contact. Refer to Fig. 2.

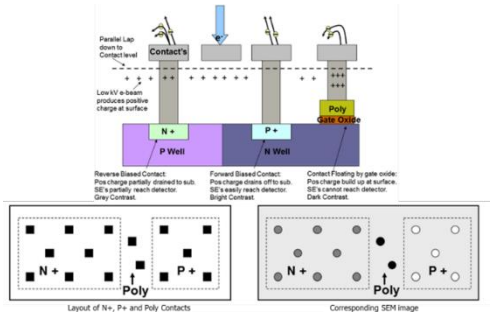



Fig. 2. PVC contrast illumination and contrast map

### *3.2.2. Nanoprobing*

Nanoprobing is a highly specialized and precise analytical technique using nanometer-scale probes to make electrical contact with, manipulate, and measure the electrical properties such as open, shorts, leakage, etc. of individual nanoscale structures of the suspected component. It enables precise and non-destructive analysis of nanoscale structures and devices.[3] Refer to Fig. 3.

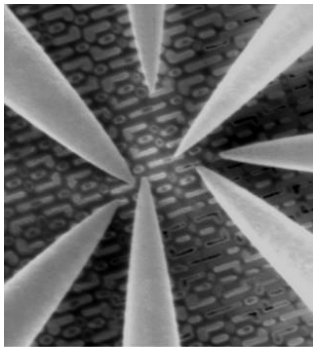


Fig. 3. Sample image of nanoprobing

### *3.2.3. Electron Beam Induced Resistance Change*

Electron Beam Induced Resistance Change (EBIRCh) is a technique requiring the use of two nanoprobes and a current amplifier. It is used to map resistance behavior of the sample by using an electron beam. To measure resistance changes, a bias is applied between the two nanoprobes and the current flowing between them is monitored while the electron beam is scanned on the sample. Whenever the electron beam induces a resistance change in the sample, the current flowing between the two nanoprobes will change accordingly and generate contrast on the EBIRCh image.[4] Refer to Fig. 4.

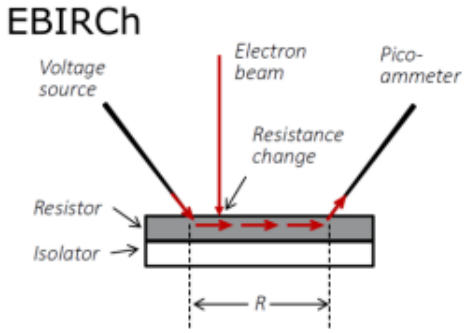



Fig. 4. Schematics of interactions between the electron beam and the sample for EBIRCh

### *3.2.4. Energy Dispersive Spectroscopy/X-ray*

Energy Dispersive Spectroscopy/X-ray (EDS/EDX) is a technique that is used to identify and quantify the elements present in a sample. It works by measuring the energy and intensity of the X-rays that are emitted by a sample when it is exposed to the electron beam of an electron microscope. Detecting and measuring these characteristic X-rays can be used to determine which elements are present in a sample and at what quantity. The left image on Figure 5 shows an incident electron from the SEM electron beam collides with an inner shell electron of an atom in the sample. This results in the emission of an inner core electron, leaving behind an inner shell vacancy. While the right image on Fig. 5 shows an outer shell electron relaxes to occupy the newly created inner shell vacancy. A characteristic X-ray, of energy hv, which is equal to the energy of the electronic transition, is emitted during the relaxation. Refer to Figure 5. [5]

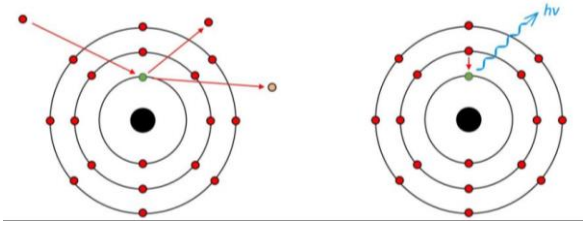



Fig. 5. Representation of how a characteristic X-ray work to show the EDS results

### *3.2.5. Transmission Electron Microscope*

Transmission Electron Microscope (TEM) uses a beam of electrons to focus on a specimen producing a highly magnified and detailed image of the specimen. When an electron illuminates the specimen, the resolution power increases increasing the wavelength of the electron transmission.[6] Refer to Fig. 6.

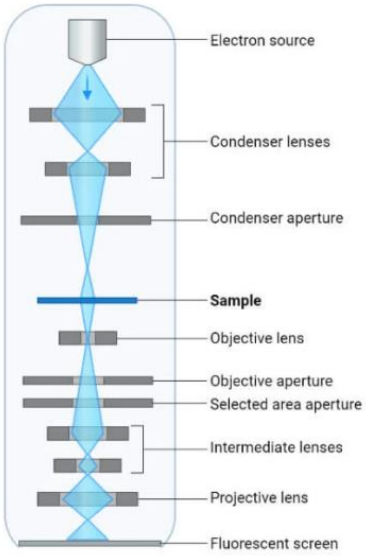



Fig. 6. Representation of how TEM works

These techniques were significant in identifying the specific location of the defect site which resulted to revealing the fabrication defect as evidenced by the Tungsten migration observed on the anomalous transistor.

## 4.0 RESULTS AND DISCUSSION

### *4.1. Summary of the Failure Analysis*

Electrical testing on the Automatic Test Equipment (ATE) deemed the Customer Returned Units (CRUs) and ILS rejects were failing quiescent current and gate voltage related test parameters. Electrical bench testing using the device-specific evaluation board showed high quiescent current and abnormal output behavior. LEM and OBIRCh post decapsulation localized anomalous emission sites and anomalous resistance changing sites, respectively. PVC analysis post mechanical delayering exhibited anomalous contrast, coinciding with the anomalous emission and resistance changing sites. Further inspection in SEM using high kilo Volt (kV) settings manifested that there was an offset on the contact plugs. Electrical Nanoprobing on a representative sample displayed a leakage from Gate-to-Source of the P-channel Metal-Oxide Semiconductor (PMOS) transistor. EBIRCh showed anomalous resistance change on Gate-to-Source channel. Physical analyses through FIB cross section, TEM, and EDS mapping revealed Tungsten (W) spur in the defect site. The analysis results have been highlighted to the fabrication site. Their investigation results revealed that the defect occurred due to a breach of the TiN barrier at the bottom of the contact. The breach can occur in rare circumstances when the contact intersects with the

spacer nitride. Critical dimension (CD) tightening was implemented at the fabrication site to address the defect.

### *4.1.1 Bench testing*

Electrical bench testing using an evaluation board was conducted. High quiescent current and abnormal output behavior was observed. See Table 1 and Fig.7.

Table 1. Quiescent current reading on a representative unit

| | Quiescent Current Failure (mA) | ATE Limit (mA) |
|---|---|---|
| Good unit | 5.5 | 5.7719 |
| Reject unit | 5.9 | |

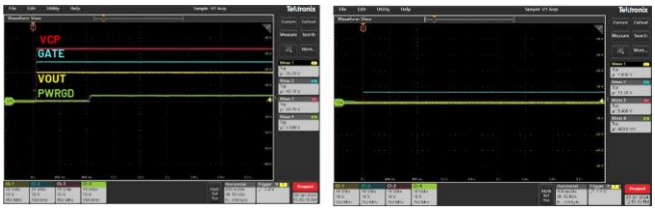



Fig. 7. Oscilloscope snapshots showing abnormal output responses on a representative reject unit

### *4.1.2. Fault Localization Post Package Decapsulation*

#### *4.1.2.1. LEM*

A cavity was created using laser in preparation for further decapsulation. Decapsulation using chemicals was done to expose the die. Photon emission analysis was performed to further isolate the location of the suspected defect, while biasing in the failing state. Anomalous photon emissions were observed. Refer to Figure 8.

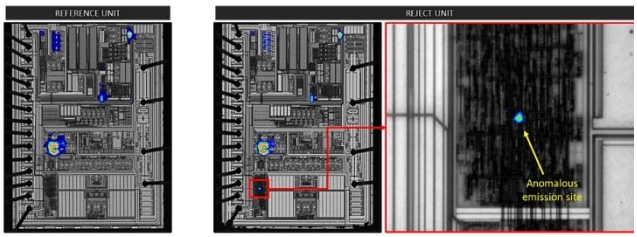



Fig. 8. LEM results of a representative unit showed a presence of anomalous emission site when compared to a known good unit

#### *4.1.2.2. OBIRCh*

The unit was analyzed using OBIRCh, while biasing the unit in the failing state. OBIRCh results showed a presence of anomalous resistance changing site when compared to a known good unit. Refer to Figure 9.

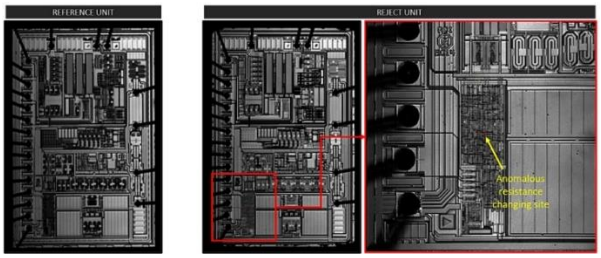



Fig. 9. OBIRCh results on a representative unit showed a presence of anomalous resistance changing site when compared to a known good unit

### *4.1.3. Chemical Deprocessing and Inspection*

One (1) unit was subjected to chemical deprocessing to expose the transistors in the silicon substrate. Pit damage sites on the edge of the gate channel was observed, see Fig. 10.1. From the initial observation, the damage looks similar to an ESD damage. A typical ESD damage is shown in Fig. 10.2. However, the damage shown in Fig. 10.1 is not an indication of an ESD damage, but a result of the tungsten spur defect. The tungsten spur has been etched away by the chemical etchant leaving pits or damage at the defect site. Chemical deprocessing was not the preferred physical failure analysis approach for this type of defect, but rather FIB cross sectioning approach to keep the defect intact.

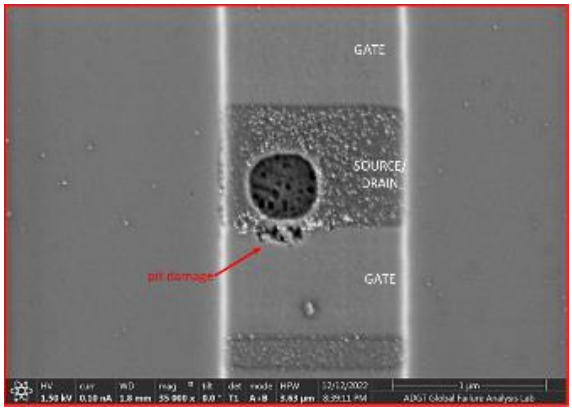



Fig. 10.1. Pit damage on the edge of the gate channel

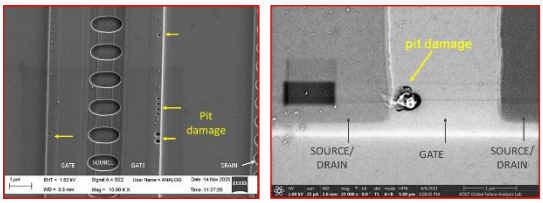



Fig. 10.2. Typical silicon pit damage on the edge and along the channel indicative of gate oxide rupture due to ESD as seen on other devices

### *4.1.4. PVC Analysis*

Several units were prepared for Passive Voltage Contrast analysis. Anomalous contrast was observed on the transistor

of digital circuitry, coinciding with the anomalous site as observed during LEM and OBIRCh. Refer to Figure 11.

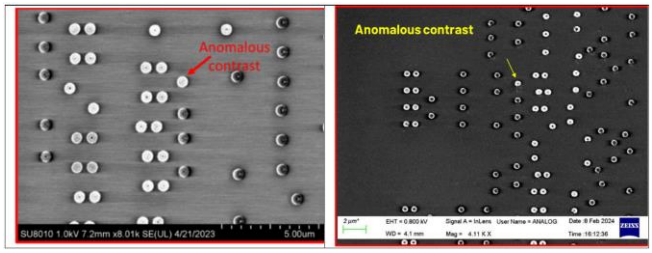



Fig. 11. Representative PVC analysis results from two failing units

### *4.1.5. Probing Analysis Post Die Extraction and Parallel Lapping*

One unit was subjected to electrical nanoprobing. A leakage from Gate-to-Source was observed on PMOS transistor. Refer to Figure 12. Misaligned contacts were also evident.

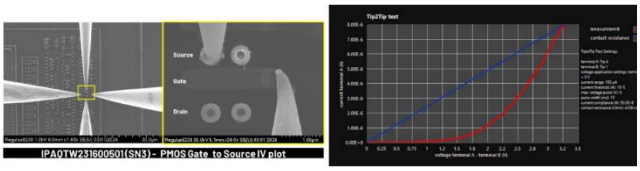



Fig. 12. Curve trace plot of Gate-to-Source PMOS transistor showing the leakage current

### *4.1.6. EBIRCh*

The unit that underwent to nanoprobing found with leakage failure was subjected to EBIRCh analysis, showing the anomalous resistance change site on Gate-to-Source channel of the suspected transistor. Refer to Figure 13.

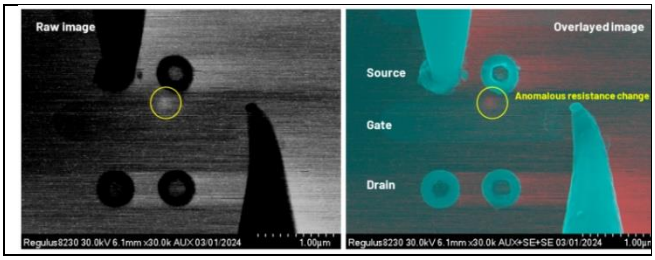



Fig. 13. Anomalous resistance change on Gate-to-Source channel was observed

### *4.1.7. Schematics and Layout Review through Avalon*

The schematics and layout through Avalon were reviewed to map the suspected component with respect to its circuit block, functionality, and electrical response based on fault localization results. Refer to Figure 14. The offset contact plugs and anomalous resistance change observed during EBIRCh were in the Sense Amplifier circuit block on the unit subjected to nanoprobing.

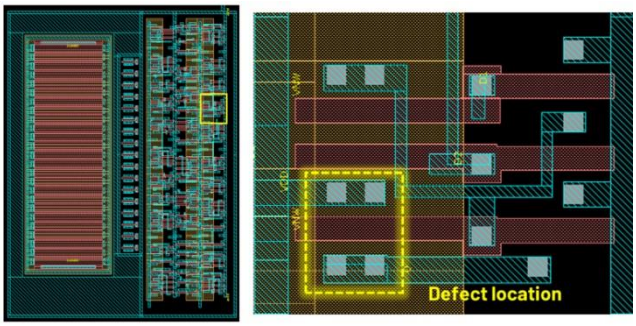



Fig. 14. Snapshot of the layout showing the location of defect

### *4.1.8. FIB Cross Section and EDS Analysis*

FIB cross section on the suspected transistor revealed an anomalous material between the Source contact and Gate of the PMOS transistor. Refer to Figure 15. EDS results revealed traces of Tungsten on the anomalous material. Refer to Figure 16.

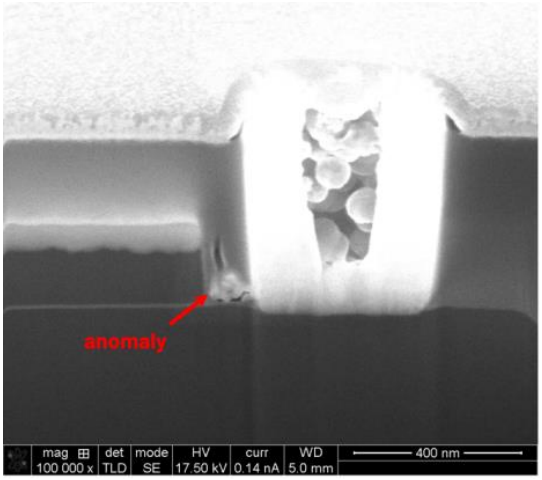
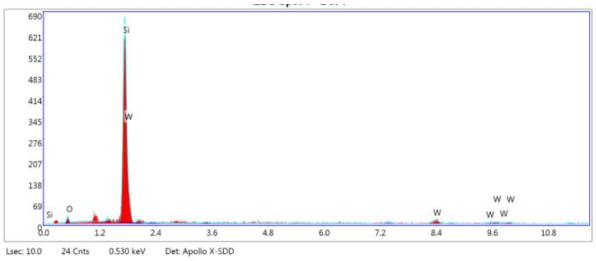



Fig. 15. SEM image showing the anomaly




eZAF Smart Quant Results

| Element | Weight % | Atomic % | Net Int. | Error % | Kratio | Z | A | F |
|---|---|---|---|---|---|---|---|---|
| O K | 3.65 | 10.13 | 13.41 | 19.66 | 0.0178 | 1.0705 | 0.4542 | 1.0000 |
| SiK | 49.76 | 78.62 | 487.95 | 3.42 | 0.4626 | 0.9849 | 0.9426 | 1.0015 |
| W L | 46.59 | 11.25 | 19.47 | 24.31 | 0.3131 | 0.6580 | 1.0214 | 1.0000 |

Fig. 16. EDS plot showing traces of Tungsten on the anomalous material

### *4.1.9. TEM and EDS Mapping*

Another representative failing unit was subjected to TEM and EDS mapping. Refer to Figure 17.

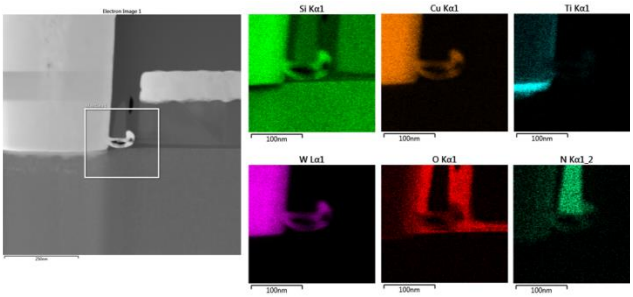



Fig. 17. EDS mapping results showing the trace of the Tungsten

## 5.0 CONCLUSION

The comprehensive failure analysis was essential for identifying the complex Gate-to-Drain/Source (D/S) Tungsten (W) spur defect. This rigorous approach incorporated advanced techniques such as Light Emission Microscopy (LEM), Optical Beam Induced Resistance Change (OBIRCh) analysis, Passive Voltage Contrast, Nanoprobing, Electron Beam Induced Resistance Change (EBIRCh) technique, and Focused Ion Beam (FIB) cross-sectioning, which were crucial for accurately pinpointing the failure mechanism.

The use of schematics and layout reviews through Avalon significantly aided in directing the subsequent fault localization steps, allowing for the isolation of the suspected block to a more specific component.

For the physical failure analysis of a Tungsten spur defect, FIB cross-sectioning was the preferred method as it prevents the defect from being etched away, unlike chemical deprocessing.

Corrective actions in fabrication, such as Poly-to-Contact Direct Measurement (WAT monitored) and reducing the Contact Critical Dimension (CD) to create more clearance, have been completed. These measures should ensure that this issue will not recur in the future.

## 6.0 RECOMMENDATIONS

The proponents recommend using the advanced techniques that will greatly add confidence to the failure analysis of the device. The schematics and layout reviews through Avalon substantially helped direct the next fault localization steps to be done to further isolate the suspected block into a more specific component. It also helped the analysis during multiple emission sites were observed that showed a common connectivity to the multiple sites. PVC pinpoints the exact transistor with anomaly on the suspected block. Further EM using high kV settings will show if there is a misalignment or a probable defect between poly and substrate layers. Nanoprobing and EBIRCh has not only showed the specific location of the defect on the anomalous component, but it greatly helped lessen the FIB cut to be done due to the concise pinpointing of the anomaly. TEM provided high-resolution images revealing the morphology and distribution of these elements within the material. This comprehensive analysis facilitated a deeper understanding of the material's properties, aiding in the identification of its origin and potential causes of leakage in integrated circuits.

## 7.0 ACKNOWLEDGMENT

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