EMPLOYING AUTOMATION OF DIRECT CURRENT RESISTANCE TESTING UTILIZING EG PROBER ON RECONSTRUCTED WAFERS FOR A COMPREHENSIVE SOLUTION OF BROKEN TRACE DETECTION AT DIE-LEVEL CIRCUITRY

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ABSTRACT

The implementation of automation in Wafer testing represents a significant leap toward enhancing efficiency, precision, and reliability. This technical paper details a comprehensive solution involving the use of an Electroglas (EG) Prober for automated Direct Current Resistance (DCR) testing on reconstructed glass wafers, aimed at detecting broken traces at the die-level circuitry its significant importance in high-volume manufacturing and possible start-up of failures at customer side. Broken traces in semiconductor devices can lead to failures, affecting the overall performance and reliability of electronic systems. Traditional methods of trace detection are often time-consuming, prone to human error, and not feasible for high-volume testing.

The EG Prober, a piece of equipment designed for high-precision electrical testing, is integrated with an automated DC resistance testing system. This integration facilitates the identification of broken traces by measuring the resistance of the circuit paths at the die level. The system employs an algorithm to analyze the resistance values, distinguishing between complete and broken traces. The use of reconstructed glass wafers in this process is particularly remarkable. These wafers provide a stable and transparent substrate (die-on-tape), allowing for enhanced visibility and access for the probing equipment. This characteristic is crucial for ensuring the accurate placement of the probe tips and minimizing the risk of further damage during the testing process. This automated solution offers several benefits over traditional testing methods. Firstly, it significantly reduces the time required for testing by automating the detection process, thus enhancing throughput in manufacturing environments. Secondly, the precision of the EG Prober ensures high accuracy in detection, reducing the likelihood of false positives or negatives that can occur with manual testing. Furthermore, this method minimizes human intervention, thereby reducing the potential for error and increasing the reliability of the testing process. Future work in this area could focus on refining the algorithm for resistance analysis, integrating artificial intelligence to improve detection capabilities, and exploring the application of this technology in other areas of semiconductor testing and manufacturing.

1. 0 INTRODUCTION

DCR testing involves selecting samples from reconstructed wafers, placing them into gel packs, and testing them manually using an offline DCR tester tool. This process, requiring manual handling of 200 dice per wafer, is not only labor-intensive but also introduces a significant yield loss. Approximately 3% of the integral yield is impacted due to these DCR samples are non-shippable. The manual process, while perhaps necessary due to the lack of automated solutions or specific testing requirements, presents several drawbacks:

- Increased Risk of Human Error: Manual handling increases the likelihood of errors, which can affect the accuracy and reliability of the testing results.
- Lower Efficiency: The manual process is time-consuming, reducing the throughput of the testing phase and potentially creating bottlenecks in production.
- Yield Loss: The requirement to use actual dice for testing, which subsequently cannot be shipped, directly affects the overall yield, contributing to wastage and increased production costs.

The implementation of an automated testing system signifies a pivotal improvement. This system automates the DCR testing process directly on the reconstructed wafer, eliminating the need for manual sample picking and handling. The benefits of this transition are multifaceted:

- Reduced Manual Handling: Automation minimizes the need for manual intervention, thereby significantly reducing the risk of human error and improving the consistency and reliability of the test results.

- Yield Recovery: Since the DCR testing can now be conducted on the wafer itself without necessitating the removal of samples, the previously considered yield loss is effectively recovered. This implies that the 3% integral yield impact seen with manual testing can be mitigated, directly enhancing overall production yield.
- Inclination to Industrial 4.0: Automated systems are generally faster and can operate continuously, increasing the throughput of the DCR testing phase. This efficiency is crucial for meeting production schedules and reducing lead times.

1.1 Background of the Study

It is noted that Product A has an FST breakdown voltage of less than 500 volts, which is lower than that of Product B. This difference in breakdown voltage indicates that Product A is more susceptible to damage from voltage spikes, potentially making it less robust against power fluctuations or ESD events. The lower breakdown voltage could be a result of differences in material properties, device architecture, or fabrication processes between the two products.

1.1.1 Customer's Power-on Failures with Product A

The observation that customer's power-on failures were noted only with Product A and not with Product B suggests that the lower breakdown voltage of Product A may be a contributing factor to its increased failure rate under normal operating conditions or during stress testing.

1.1.2 Failure Analysis and Cause

The FA concluded that the failure in Product A was due to a broken copper (Cu) trace, consistently found near the non-active pads. This location, being susceptible to mechanical stress or electrical overload, is highly suspected to have been compromised by an ESD event. Refer to Figures 1 to 3.

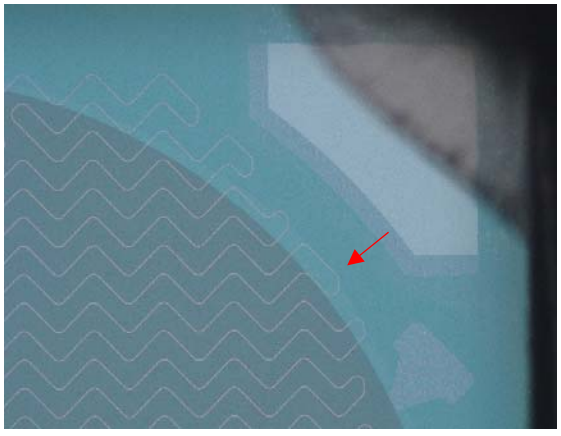


Figure 1: Broken Trace Location 300x magnification

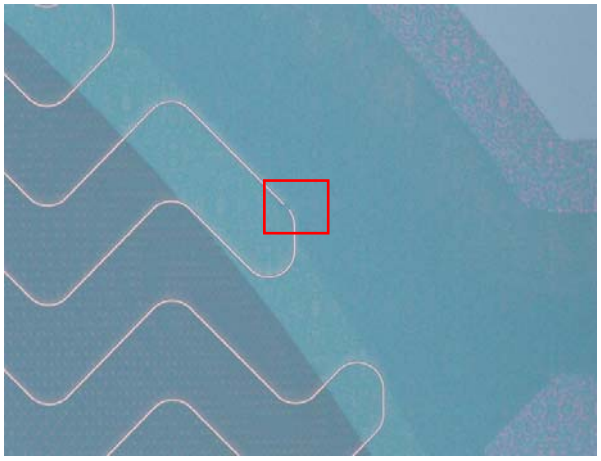


Figure 2: 1000x magnification Broken trace length

Figure 3: 1500x magnification of Broken trace length

1.2 ESD Mapping and Fault Injection

Despite the suspicion of an ESD event causing the failure, ESD mapping across all process steps did not reveal any event that exceeded Product A's breakdown voltage. This suggests that either the ESD mapping was not sufficiently sensitive to detect all relevant ESD events or that the breakdown voltage of Product A is lower than previously estimated, or it may indicate that cumulative sub-threshold ESD events could contribute to the observed failures.

Replicating the defect through fault injection by processing without proper grounding (lack of wrist strap and ESD shoes covered with blue tape) successfully recreated the defect observed in FA. This experiment underscores the critical importance of strict adherence to ESD protection protocols during manual handling and processing. The matching signatures of the artificially induced defect and the defect found in failed Product A units confirm the role of ESD as a causative factor.

1.3. Review of the Current Process State

The current gap in testing and methodology underscores the need for an innovative approach that can enhance the detection of broken traces at the die-level circuitry without compromising the efficiency, accuracy, and throughput of the testing process aside from the traditional Manual DCR testing. The deployment of automated DCR testing utilizing an EG Prober on reconstructed glass wafers presents a promising solution. However, this approach requires thorough investigation to validate its effectiveness, understand its limitations, and determine its practicality for widespread adoption in wafer testing. The problem, therefore, centers on evaluating the viability and benefits of employing automation in DCR testing on reconstructed glass wafers as a comprehensive solution for broken trace detection, aiming to overcome the limitations of manual testing methods and improve the overall quality and reliability of semiconductor devices.

1.4 Objective of the Study

The objectives of the study are specifically shaped to highlight the distinctions, advantages, and potential limitations of employing an automated system for the detection of broken traces in die-level circuitry. These objectives include:

- *Compare the Accuracy of Automated vs. Manual DCR Testing.* Assess and quantify the precision and reliability of automated DC resistance testing in identifying broken traces within die-level circuitry on reconstructed glass wafers, as compared to the accuracy achievable through manual testing methods.

- *Evaluate Efficiency and Throughput Differences.* Analyze the impact of automation on the efficiency and throughput of the DC resistance testing process. This involves comparing the time required to test a specific number of wafers using automated methods (utilizing the EG Prober) against the time needed for equivalent manual testing efforts, thereby highlighting potential improvements in testing speed and operational productivity.
- *Assess Yield Impacts from Testing Methodology.* Determine how each testing approach affects the overall yield of semiconductor manufacturing. This objective looks at the potential yield recovery or enhancement through the reduction of handling errors, contamination risks, and improved detection of defects afforded by automated testing, in contrast to the yield implications of continuing with manual testing practices.
- *Investigate Handling and Operational Risks.* Examine the differences in handling and operational risks between automated and manual DCR testing, particularly focusing on the susceptibility to human error, the potential for physical damage to wafers during handling, and the risk of electrostatic discharge (ESD) event.

1.5 Scope and Limitations

The scope and limitations of this study are outlined as follows:

- The study focuses on evaluating the technological aspects of automated DC resistance testing using an EG Prober against traditional manual testing methods, specifically in detecting broken traces at the die-level circuitry on reconstructed glass wafers.
- The study includes a thorough examination of the efficiency and throughput of the automated testing process in comparison to manual methods, highlighting potential improvements in operational speed and productivity.
- An assessment of how automated and manual DCR testing methods influence the overall yield of semiconductor manufacturing, considering factors such as yield recovery and the prevention of additional defects through handling.

2.0 REVIEW OF RELATED WORK

Detecting broken traces at the die level in circuits is crucial to assuring the integrity and functionality of devices. DCR testing is a general approach for detecting defects since it is simple and effective. DCR testing involves applying a small DC voltage across a circuit and measuring the resulting current flow [1]. The resistance is then calculated using Ohm's Law (Resistance = Voltage / Current). In the context of semiconductor manufacturing, this technique is used to verify the electrical continuity and integrity of metal traces within a die. Broken or defective traces exhibit higher resistance values or complete open circuits, deviating from expected norms for a properly functioning device [2].

In semiconductor manufacturing, ensuring the integrity of metal traces at the die level is paramount for device reliability. Broken traces can lead to device failure, affecting everything from basic electronic functions to the performance of complex integrated circuits. The literature highlights several key points regarding the application of DC resistance testing:

- *Sensitivity and Precision:* The sensitivity of DC resistance testing allows for the detection of even minute changes in resistance, making it suitable for identifying subtle defects that might not be visually apparent or detectable by other means [3].
- *Non-Destructive Testing:* As a non-destructive method, DC resistance testing can be performed without damaging the device, making it ideal for quality control

processes where devices need to be preserved for further steps in manufacturing or for sale.
- *Automation and Throughput:* With advancements in testing equipment and automation, such as the use of EG Probers, manufacturers can conduct DCR tests with high throughput, integrating this testing phase seamlessly into the production line. Automation reduces the likelihood of human error and increases the consistency of testing outcomes.

While DC resistance testing is highly effective, it is not without its challenges. The literature identifies several areas of concern and potential solutions:

- *Detecting Very Small Defects:* As circuits become more densely packed and trace widths decrease, detecting very small defects becomes increasingly challenging. Advances in testing technology, including higher sensitivity instruments and improved algorithms for data analysis, are critical for addressing this issue.
- *Differentiating Between Defect Types:* DC resistance testing primarily identifies electrical discontinuities but may not always distinguish between different defect types (e.g., a complete break vs. a partial crack). Combining DCR testing with other methods, such as optical inspection or acoustic microscopy, can provide a more comprehensive understanding of the defect [4].
- *Adapting to New Materials and Structures:* With the introduction of new materials and three-dimensional (3D) structures in semiconductor devices, adapting testing methods to these innovations is necessary. Ongoing research and development efforts focus on modifying existing testing techniques and developing new protocols to accommodate these changes [5].

DCR resistance testing plays a crucial role in identifying broken traces at the die level, ensuring the reliability and performance of semiconductor devices. As highlighted in the literature, ongoing advancements in testing technology and methodologies are essential to address the evolving challenges presented by modern semiconductor manufacturing [6]. Combining DCR testing with other diagnostic methods and leveraging automation can enhance defect detection capabilities, contributing to higher quality and more reliable electronic products.

3.0 METHODOLOGY

3.1 Research Design

This study employs a comparative experimental research design to thoroughly evaluate the impact of automation in DCR testing on the accuracy, efficiency, and yield enhancement in detecting broken traces at the die level within semiconductor circuitry. The focus on employing an EG Prober for automated testing, contrasted with conventional manual testing methods, aims to provide a comprehensive understanding of how automation can revolutionize quality assurance processes in wafer testing.

The methodology is grounded in a quantitative analysis framework as shown in Appendix – A, allowing for the objective measurement of testing accuracy, throughput, operational efficiency, and yield impact. By systematically collecting and analyzing data from both automated and manual DCR testing processes, the research seeks to illuminate the differences in performance, highlighting the advantages and potential limitations of automation in this critical aspect of production.

The study delineates the specific configurations of the automated testing setup using the EG Prober, alongside the parameters set for manual testing, ensuring that both processes are comparable in terms of testing conditions and objectives. A stratified sampling approach is utilized, selecting a diverse range of reconstructed glass wafers with embedded die-level circuitry. This ensures a broad representation of potential challenges encountered in DCR testing, enhancing the generalizability of the findings. Detailed data collection is established, focusing on key metrics such as detection accuracy testing throughput (time per wafer), and operational efficiency. Additionally, data on yield impact, in terms of defect detection and handling-induced failures, are systematically gathered.

The methodology incorporates analysis techniques to rigorously compare the outcomes of automated and manual DCR testing. To ensure the reliability and validity of the testing processes and data analysis, the study employs calibration checks, equipment validation protocols, and inter-rater reliability assessments for manual testing processes.

3.2 Manual DCR Testing Methodology

The manual DCR Testing is being handled by PC Inspector publishing the result. Flow of operations is indicated at Figure 5.

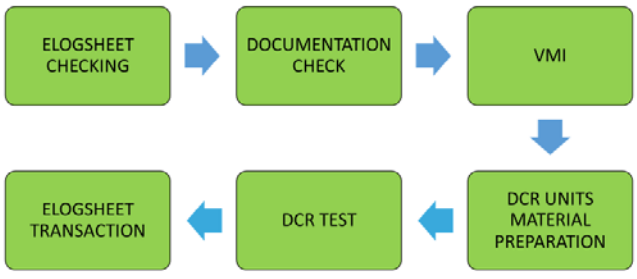


Figure 4: Current state of Manual DCR Testing handled by PC

PC Inspector is using the Monitor interface with specialized software intended for Manual DCR Testing. Below is the user interface of PC in performing the Manual DCR Testing.

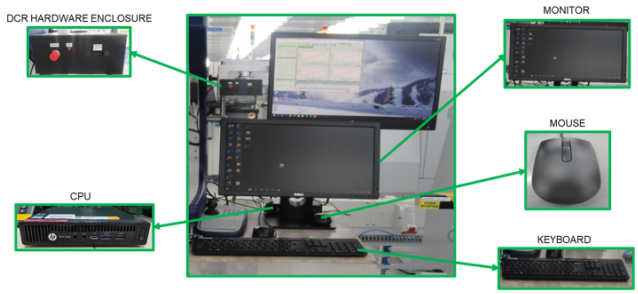


Figure 5: Interface of PC in performing Manual DCR Testing.

Unit per unit, PC patiently transfers the die on the board to perform manual Testing

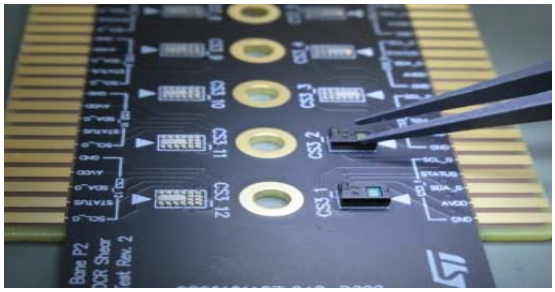


Figure 6: Manual Placement of unit

3.3 Automated EWS Reconstructed Wafer Setup Overview

The adoption of Automated DCR Testing involves the utilization of specialized machinery. The EG Prober 4090f+ is a key piece of equipment identified for its ability to meet these requirements [7] and facilitate the transition to automated processes.

Figure 7: EG Prober 4090F+

3.4 Test Flow, Specifications and Binning

The Test flow executes a predefined sequence of electrical tests across the wafer, applying a direct current through the circuitry and measuring the resistance at multiple test points. Data from each test point is collected in real-time and analyzed by the system software to identify discrepancies indicative of broken traces or defects. Below is the binning and Soft Bin description identified for the Auto DCR Testing using Reconstructed Wafer in EG-Prober. Soft Bin Identification are indicated in Appendix -B.

Upon completion of DCR testing, wafers are categorized into bins based on the detected electrical properties and the presence of defects.

3.5 Auto DCR Test Plan

This plan is structured to maximize the efficiency, accuracy, and reliability of the testing process, utilizing advanced equipment such as the EG Prober 4090f+. This is automatically categorize dice into bins based on the outcome of DCR tests, separating those that meet quality standards from those with detectable defects as shown in Appendix - C.

3.6 Control Maps for DCR Sampling

The implementation of Automated DCR Testing requires a structured approach to DCR sampling to ensure comprehensive and efficient defect detection within die-level circuitry. Automated DCR Control Maps serve as a pivotal tool in this process, guiding the sampling strategy and ensuring that testing is both thorough and optimized as shown in Appendix - D

3.7 Probing Process Capability

In automated DCR testing, the probing process involves the precise engagement of probe needles with specific points on the semiconductor wafer to measure electrical resistance. This is essential for detecting minute anomalies in die-level circuitry that could indicate potential defects.

Precision Alignment: The automated system, such as the EG Prober 4090f+, must ensure ultra-precise alignment of probes to test points. This involves sophisticated optical and mechanical positioning systems capable of sub-micron accuracy to avoid misalignment errors and ensure consistent contact quality.

Contact Integrity: Maintaining optimal electrical contact between the probe and the circuitry during testing is crucial. The system must monitor and adjust for contact resistance in real-time, ensuring reliable resistance measurements across all test points.

Minimal Mechanical Stress: The probing mechanism should apply minimal mechanical stress on the wafer to prevent damage. This requires the integration of advanced load control technology within the prober to regulate the force exerted by probe needles.

3.8 Loop Run Test

Loop testing in DCR sampling involves the systematic application of a direct current through specific circuit loops or paths within a die to measure and analyze the resistance. This method is pivotal for pinpointing resistance anomalies that may indicate broken traces, shorts, or other forms of electrical discontinuities, which are crucial for maintaining the integrity and functionality.

4.0 RESULTS AND DISCUSSION

4.1 Probing Process Capability Result

A total of 40 sample dice, divided into 4 distinct sets, each comprising 10 sample dice is used for the Probing Process Capability. This subdivision allows for a controlled and comparative analysis across different operational conditions. The sample dice are likely chosen based on specific criteria to represent a variety of circuit layouts, defect types, or manufacturing processes to ensure the findings are robust and broadly applicable. Utilizing multiple sets of samples enhances the reliability of the test results by providing sufficient data points for statistical analysis and mitigating the impact of outliers or anomalous readings as shown in Appendix – E.

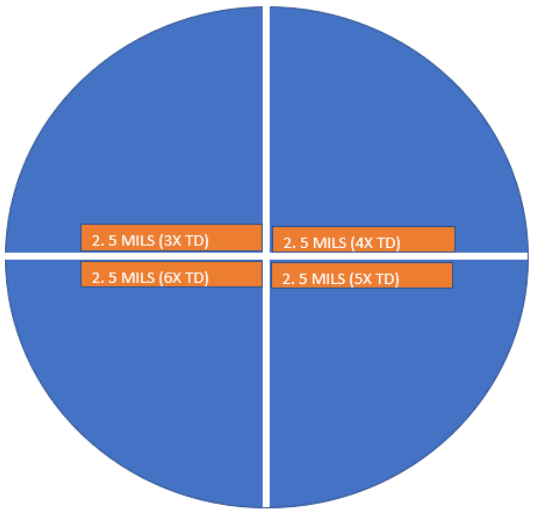


Figure 8: Location of each set of sample dice on the wafer

During the Visual Mechanical Inspection (VMI), it was noted, as anticipated, that there were several probe impressions on the pad. Importantly, no damage to the pad was detected. Die images after VMI are shown in Appendix – F.

4.2 Loop Run Test Result

The Electrical Wafer Sort (EWS) Recon Resistance to Failure Time Constant (RFTC) test yielded an average resistance value of 14,733 ohms. This specific measurement pertains to a characteristic such as contact resistance or path resistance within the circuitry of the die, is critical for evaluating the electrical properties of the die. Variation of +/- 1 ohm underscores the high degree of precision achieved in the testing process. Such minimal variation is indicative of a highly stable testing suggesting that the measurement technique is both accurate and reliable.

A slightly higher variation of approximately +/- 1.5 ohms in the Machine RFTC measurements suggests a minor increase in the variability of results in a different set or iteration of tests. While still within a narrow range, this variance is critical for understanding the limits of the test's precision and identifying potential areas for improvement of the testing process and the equipment used. Difference in Loop Test in Machine 3 and Machine 1 is as shown in Appendix – G.

4.3 GRR Run Result

The GRR shows the variance contributions from different test parameters, namely repeatability and reproducibility The results indicate that most of the measurement variance can be attributed to the actual differences among the items being measured, rather than to inconsistencies in the measurement system. The outcome shows a positive response and accepts upon review of the GRR limit and GRR results and measurements were shown in Appendix – H.

4.4 Machine 1 vs Machine 3_Recon Correlation Run

90 dice are tested in Auto DCR setup and correlate the RFTC test results with Machine 1 setup. Result showed that Machine 3 RFTC measurement is a bit higher compared to Machine 1 see Appendix – I. Comparing to Manual DCR tester, Auto DCR setup has much better correlation with respect to Machine 3.

Auto DCR RFTC drift ranges from 65.25 ohms to 84.54 ohms. This drift is much lower compared to the RFTC first observed in Manual DCR tester, which around +/- 1k ohms

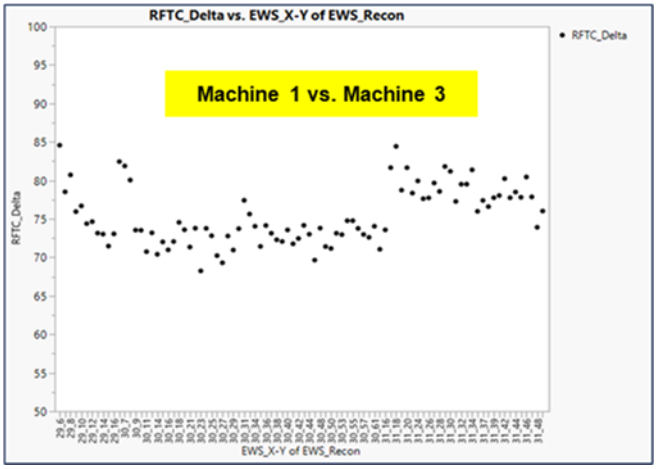


Figure 9: Machine 3 vs Machine1 Correlation RFTC Delta

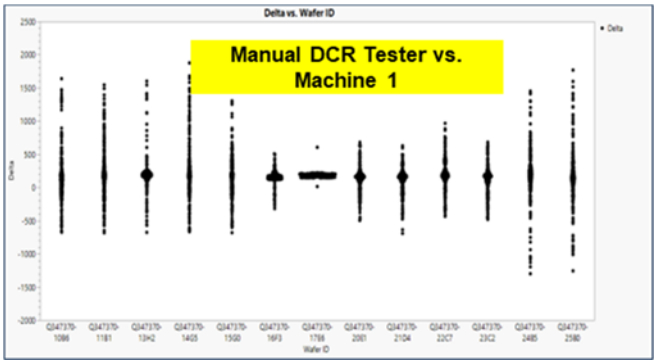


Figure 10: Correlation on Manual DCR Tester and Machine 1

Machine 3 average RFTC is 15796.9 ohms vs Machine 1 average RFTC of 15721.5. The average delta is 75.4 ohms.

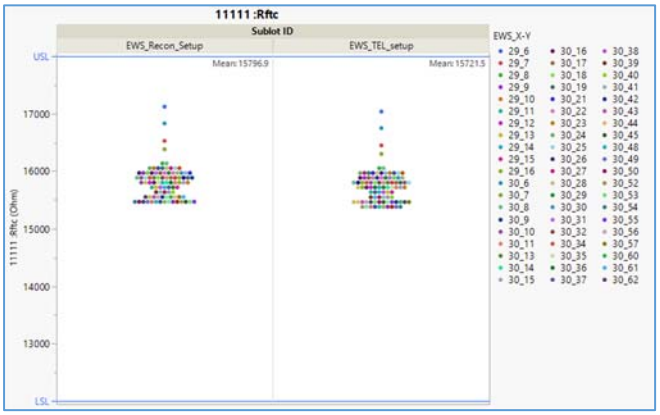
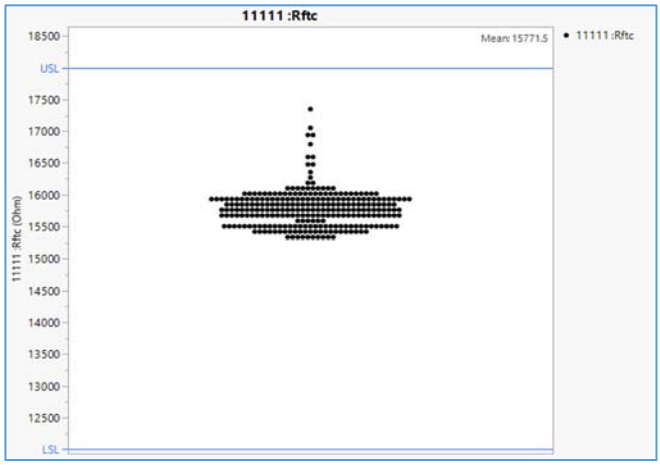


Figure 11: RFTC comparison between Machine 3 and Machine 1

4.5 Actual Run using Auto DCR

There were 240 sampling test result is 100% passing. Some dice have tailing RFTC measurements to USL, the same performance in Machine 1 for this wafer.



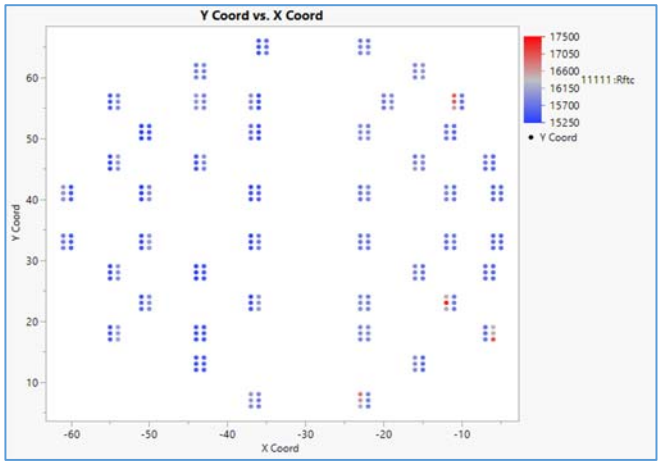


Figure 12: Bin Failure topography on Wafer Map (DCR Sampling for Product A)

Recon Wafer full wafer run yields 99.83%. There are dice are all continuity test (open fail). Failure is confirmed valid after retest.

HBin	SBin	First Failed Test	N Rows	% of Total
2	2		3436	99.83%
5	501	Cont_Verf_Pad3_Param	5	0.15%
5	505	Cont_Verf_MP1_Param_5V	1	0.03%

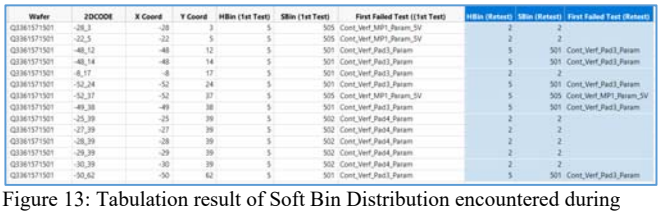


Figure 13: Tabulation result of Soft Bin Distribution encountered during Auto DCR

4.6 Time Study of Auto DCR through Full Test and Sampling

The Time Study conducted has yielded comprehensive results, demonstrating significant efficiency gains and operational effectiveness in the testing process.

The Units Per Hour (UPH) for a complete test stands at 3,401, whereas for sampling, it reaches 11,436. These notable numbers have established sampling testing as the suitable strategy for DCR testing. The dice that are tested form part of the quantity that can be shipped and will not be discarded as shown in Appendix – J.

4.7 Auto DCR Testing Result

DCR samples (200pcs per lot) from 25 wafers are tested in Manual DCR tester. 100% passing result on all wafers. DCR readings are within 12k to 18k ohms limit shown in Appendix - K.

Machine 1 RFTC average measurements are 13479 ohms vs Manual DCR average RFTC of 13301.9. The average delta is 168.1 ohms. Correlation is observed between Machine 1 and Machine 3, but some samples are drifting +1500 ohms to -1000 ohms which were shown in Appendix – L.

4.8 Grounding and ESD Checking

Auto DCR setup is properly grounded and Resistance checks are within expected value.

Stage	SPECS	Measurements	
Chassis to common point	< 1 MOhm	1.0ohm	
Loader/Unloader(moving)	< 1 MOhm	542ohms	
Robot Arm(moving)	< 1 MOhm	2.7ohms	

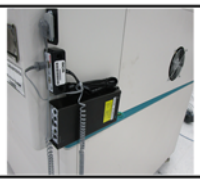
Stage	Checks	
Ground strap monitor		
Machine grounding to common point		

Figure 14: Proper ESD and Grounding feature on EG-Prober to accept the implementation of Auto DCR Testing

5.0 CONCLUSION

Furthermore, the comparative analysis between Manual DCR Testing and Automated DC Resistance Testing using an EG Prober illuminates several critical distinctions in efficiency, accuracy, scalability, and overall impact on semiconductor manufacturing processes. This detailed conclusion draws upon various dimensions of comparison to elucidate the advantages and limitations of each approach.

In terms of Efficiency and Throughput, Manual DC resistance testing is inherently time-consuming due to the need for individual setup and measurement by technicians. This labor-intensive process leads to longer test cycles per wafer, limiting the throughput and creating bottlenecks in high-volume manufacturing environments. While it allows for flexibility and immediate human judgment, the speed at which manual testing can be conducted is significantly slower, affecting overall production timelines. Also, the accuracy of manual testing is highly dependent on the skill and experience of the operator, which can lead to variability in results. Manual alignment and contact errors can introduce additional resistance, affecting the precision of the measurements. Furthermore, the potential for human error in recording and interpreting results can compromise reliability. However, implementing Automated DC Resistance Testing will significantly reduce the time required for each measurement. Automated testing systems can operate continuously without fatigue, dramatically increasing throughput. The automated setup eliminates manual handling errors, streamlines the testing process, and allows for the simultaneous testing of multiple sites, further enhancing efficiency. Automation minimizes human error, ensuring consistent and precise placement of probes and standardization of the testing procedure. The EG Prober's sophisticated software and hardware are designed to achieve high accuracy in resistance measurement, with advanced algorithms that can detect subtle anomalies indicative of broken traces or other defects. This precision enhances the

reliability of the testing process, providing a solid basis for quality assurance.

Automated testing not only addresses the limitations inherent in manual testing but also aligns with the industry's move towards precision manufacturing and high-volume production. The transition to automation is not without its challenges, including initial cost and the need for technical expertise to operate and maintain the equipment. However, the long-term benefits of incorporating automated DC resistance testing into Wafer Testing manufacturing processes are clear, setting the way for advancements in quality, efficiency, and innovation in the field.

6.0 RECOMMENDATIONS

A key recommendation to enhance and expand upon this foundational work involves the integration of adaptive testing protocols powered by data analytics and machine learning (ML) technologies. This approach aims to optimize testing efficiency, accuracy, and scalability, thereby addressing some of the key challenges faced by the semiconductor industry today.

Leverage ML algorithms to analyze test data in real-time, enabling the automated testing system to adaptively modify testing parameters and strategies based on the detection of patterns indicative of potential defects.

Through Data Collection and Preprocessing, it can implement a systematic data collection framework that captures a comprehensive dataset from the DC resistance tests, including resistance values, test duration, probe contact stability, and any anomalies encountered during testing. Also need to Develop ML models that can analyze the collected data to identify patterns or signatures associated with broken traces or other types of defects. These models should be capable of continuously learning and improving their predictive accuracy over time. Integrate the ML models into the EG Prober's control software, enabling the system to utilize the models' insights to dynamically adjust testing parameters. For example, if the model predicts a high likelihood of trace defects in a particular area of the wafer, the system could automatically adjust the testing resolution or sensitivity in that area. Establish a real-time feedback loop where the testing system can adjust its testing strategy based on the ML models' recommendations. This includes modifying the testing path, altering the electrical testing parameters, and even changing the sequence of tests to prioritize areas with a higher likelihood of defects. Regularly validate the ML models against known outcomes to ensure their accuracy and reliability. Use these validation exercises as opportunities to refine and improve the models, incorporating new data and insights to enhance performance.

Following the implementation stages above:

1. *Increased Testing Efficiency:* Concentrating on regions with a greater probability of defects streamlines the testing procedure, decreasing the total duration of tests and enhancing production capacity.
2. *Improved Accuracy:* Customizing testing parameters to match the unique attributes of each wafer enhances the precision in identifying broken traces and other anomalies.
3. *Scalability:* A machine learning-enhanced adaptive testing approach can flexibly expand to suit various wafer types and defect configurations, establishing it as a multifaceted asset in the semiconductor production workflow.
4. *Cost Reduction:* Improving the efficiency and precision of testing can result in considerable cost reductions by minimizing the quantity of wafers that require retesting or elimination because of unnoticed flaws.

7.0 ACKNOWLEDGMENT

The successful completion of the research project titled "Employing Automation of Direct Current Resistance Testing Utilizing EG Prober on Reconstructed Glass Wafers for A Comprehensive Solution of Broken Trace Detection at Die-Level Circuitry" was made possible through the support and contributions of various individuals and organizations. We extend our heartfelt gratitude to all those who played a pivotal role in the realization of this work.

Firstly, we would like to acknowledge the support received from the Division headed by Omar Santos whose generosity of test product expertise and resources are shared for this research. His commitment to advancing technological research has been invaluable to our endeavors.
Special thanks are due to the team of Equipment Team headed by Wendell Beatingo. for providing the EG Prober equipment and for their technical support throughout the project. Their expertise and willingness to assist with the intricacies of the equipment were critical to the success of our testing procedures.

Secondly, we would like to thank the support coming from the Management Team, especially to Ma'am Aileen Gonzales for their unwavering sponsorship and encouragement. Their belief in our capabilities has been a source of motivation and resilience during the demanding phases of this project.

This research is a testament to the power of collaboration and support across different spectrums of the academic and industrial community. We are grateful for the opportunity to contribute to the field of manufacturing and testing and look forward to the potential applications and future developments arising from this work.

8.0 REFERENCES

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9.0 ABOUT THE AUTHORS

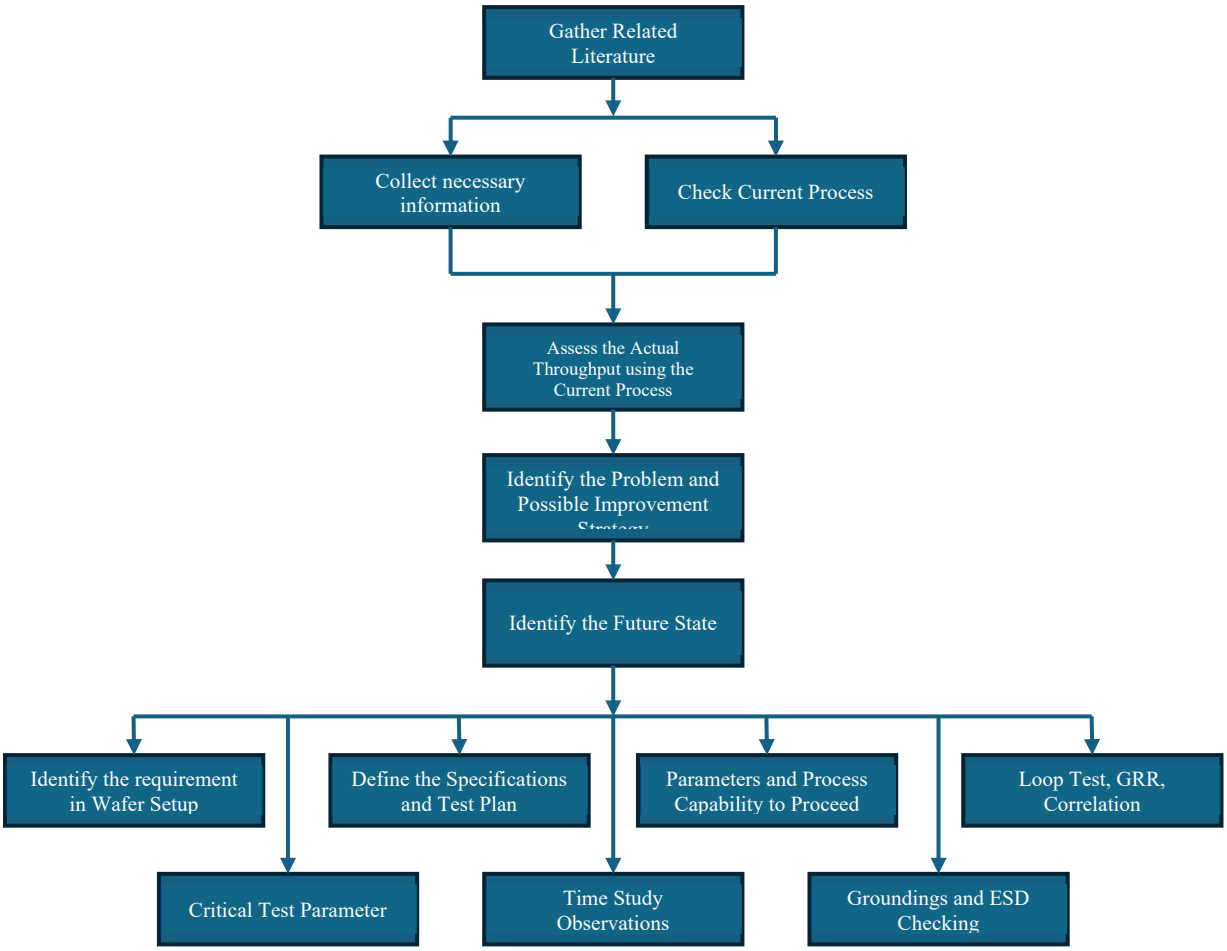
Bryan M. Delos Santos holds a degree in Electronics Engineering with extensive practical knowledge in the Wafer Probing Industry. He's been with STMicroelectronics for 2 years as Test Process Engineer 2 which continues to enhance analysis and interpretation and provides a comprehensive, well-rounded perspective.

Richelle D. Barcarse is a Senior Technician at STMicroelectronics and has a degree in Electronics Technical Course. The study's discussion and recommendations provide more in-depth analysis and comprehension through her valuable knowledge and vast hands-on involvement in the Wafer Test processes.

Judioz M. Manejero is currently a Process Engineering Manager in STMicroelectronics and managing the Wafer Test, Final Test and Finish Process area. He received his Bachelor of Science Degree in Electronics and Communications Engineering from Mapua University in Intramuros, Manila.

10.0 APPENDICES

Appendix – A: Research Design for the Implementation of Automated DCR Testing using EG-Prober



Appendix – B: Soft Bin Identification for Automated DCR Testing using EG-Prober

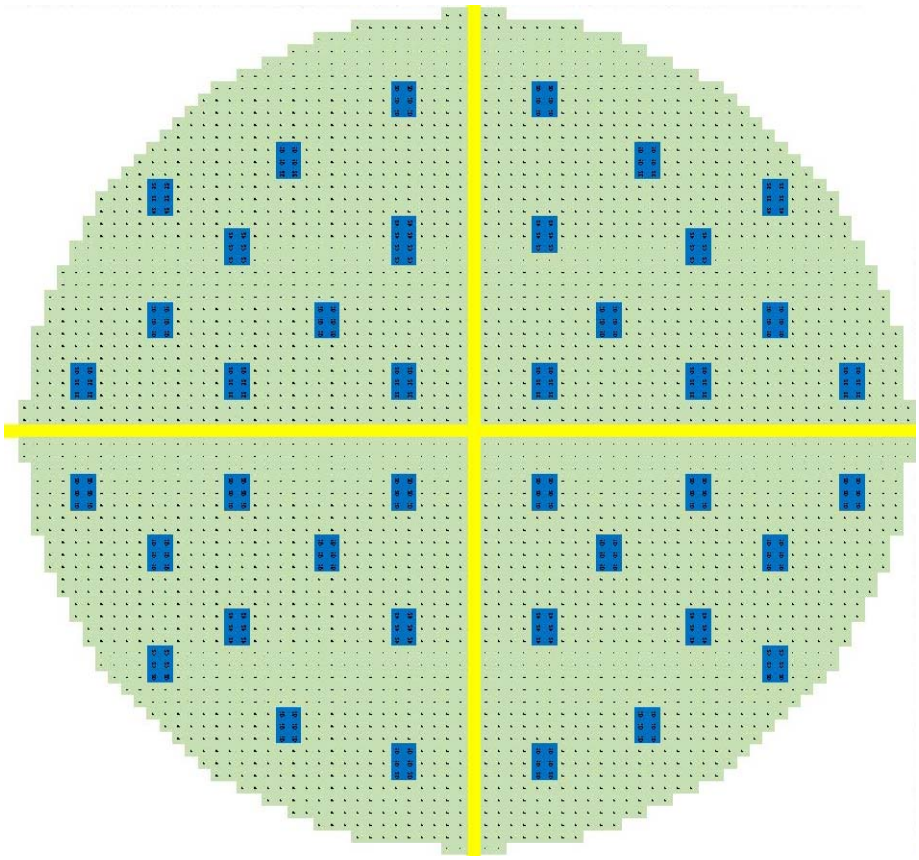
Test id	Name	Th Low (Prod.)	Th High (Prod.)	Units	Pass Bin (HwBin)	Fail Bin (HwBin)
3111	Cont_Verf_Pad3_Param	4	6	V	2 (2)	501 (5)
4111	Cont_Verf_Pad4_Param	4	6	V	2 (2)	502 (5)
4112	Cont_Verf_MP1_Param_5V	4	6	V	2 (2)	505 (5)
4113	Cont_Verf_MP2_Param	4	6	V	2 (2)	505 (5)
4114	Cont_Verf_MP1_Param_2V	1	3	V	2 (2)	505 (5)
5111	Test_Time_Cont			mSec	2 (2)	5 (5)
9113	Leak_Verf_Pad1_Main_Pad3	0		uA	2 (2)	503 (5)
9114	Leak_Verf_Pad1_Main_Pad4	0		uA	2 (2)	504 (5)
10121	Info_Shunt_Current	140	160	uA	2 (2)	506 (5)
11111	Rftc			KOhm	2 (2)	511 (5)
12111	Test_Time_Res			mSec	2 (2)	5 (5)
14111	Info_MP1_V1	0		V	2 (2)	509 (5)
14112	Info_PShunt_V3	0		V	2 (2)	508 (5)
15111	Info_MP2_V2	0		V	2 (2)	510 (5)
15112	Info_NShunt_V4	0		V	2 (2)	507 (5)

Appendix – C: Test Parameters used for Auto DCR using EG Prober

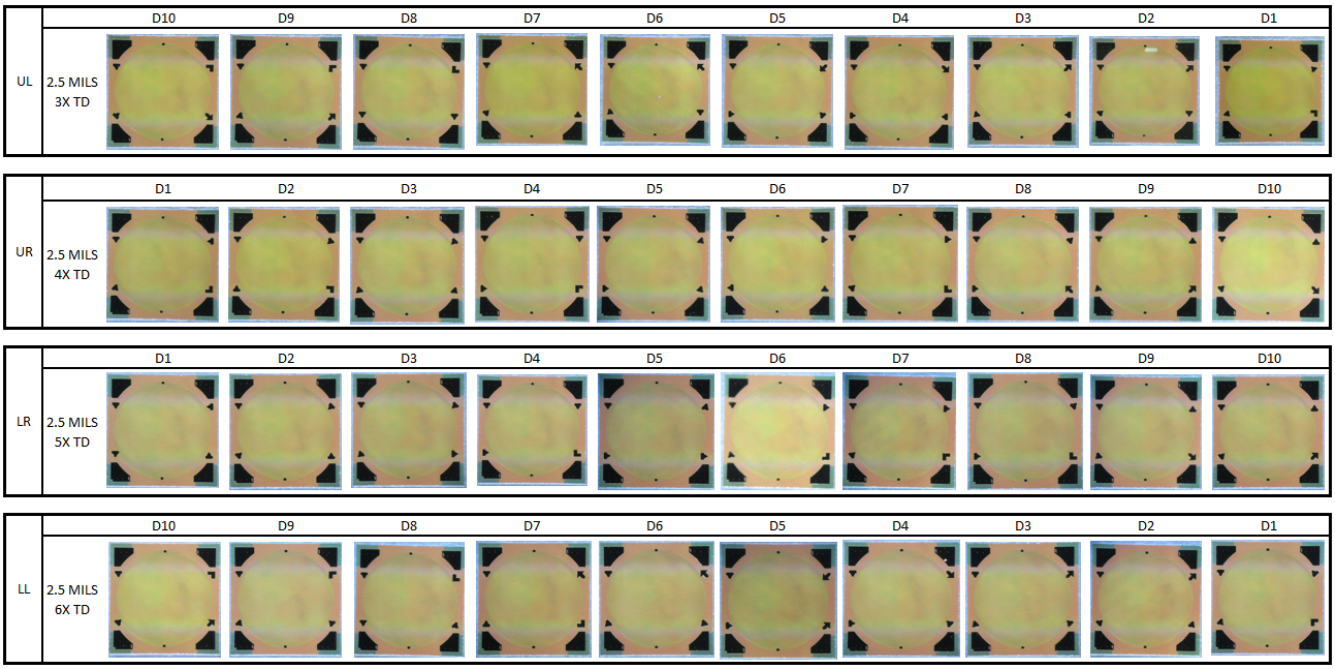
TEST PARAMETER	DEFINITION	FORCE	MEASURE	EXPECTED WHEN OPEN	EXPECTED WHEN SHORT
Cont_Verf_Pad3_Param	Parametric check for contact on both Force and Sense Pins on Verify Pad 3	5.0V on VP4_F using Analog Pin	Voltage on VP4_S FVMV (FV 1.0V)	1.0 V	4.8 V
Cont_Verf_Pad4_Param	Parametric check for contact on both Force and Sense Pins on Verify Pad 4	5.0V on VP4_F using Analog Pin	Voltage on VP4_S FVMV (FV 1.0V)	1.0 V	4.8 V
Cont_Verf_MP1_Param_5V	Parametric check for contact on Main Pad pin MP1_F	5.0V on MP1 using Analog Pin	Voltage on MP1 (Same Pin Electronic FVMV)	Floating value ~ 3V	5.0 V
Cont_Verf_MP2_Param	Parametric check for contact on Main Pad pin Pshunt	300uA on MP1_F using Analog Pin [Range:512uA]	Using Pshunt, Force 2.0 V Measure Voltage [Range:6.5V]	Open Pshunt connection , ~ 0.47 V	~ 2.77 V
Cont_Verf_MP1_Param_2V	Parametric check for contact on Main Pad pin MP1_F Due to tester limitation getting floating value when sense is floating, another test with another Voltage value needed to confirm contact	2.0V on MP1_Force using Analog Pin [Range:6.5V]	Voltage on MP1_F (Same Pin Electronic FVMV)	Floating value ~ 3.0 V	2.0 V
Leak_Verf_Pad1_Main_Pad3	Short Detect Trace vs Fail Safe Trace short test Check for short between Verify Pad 3 vs Main Pad Need to check for open connection	0.0V on MP1_F using Analog Pin [Range:32mA] 5.0V on VP3_S [Range:6.5V]	Current on VP3_S	In the range of nA to fA	In the range of ~ 22uA
Leak_Verf_Pad1_Main_Pad4	Check for short between Verify Pad 4 vs Main Pad (SDT vs FST short test) Need to check for open connection	0.0V on MP1_F using Analog Pin [Range:32mA] 5.0V on VP4_S [Range:6.5V]	Current on VP4_S	In the range of nA to fA	In the range of ~ 22uA
Info_Shunt_Current	Parametric check for current passing through the 10k Shunt Resistance			Ideally ~ 0 A ; actual value on V3 and V4 is	

	Control to check for accuracy/drift of the 10k shunt resistor The difference between voltage Pshunt (V3) and Nshunt (V4) divided by Rshunt value (9.999k ~10K)			not zero (0) but very small values close to zero, thus we expect current in the range of nA.	
Rftc	Resistance check of the Fail Safe Trace between MP1 and Pshunt Rftc = (V1-V2) / Current Shunt	300uA Current on MP1_F using [Range:512uA]	Voltage on MP1_S (V1), MP2_F (V2), Pshunt (V3), Nshunt (V4) Current Shunt = (V3-V4) / Rshunt		

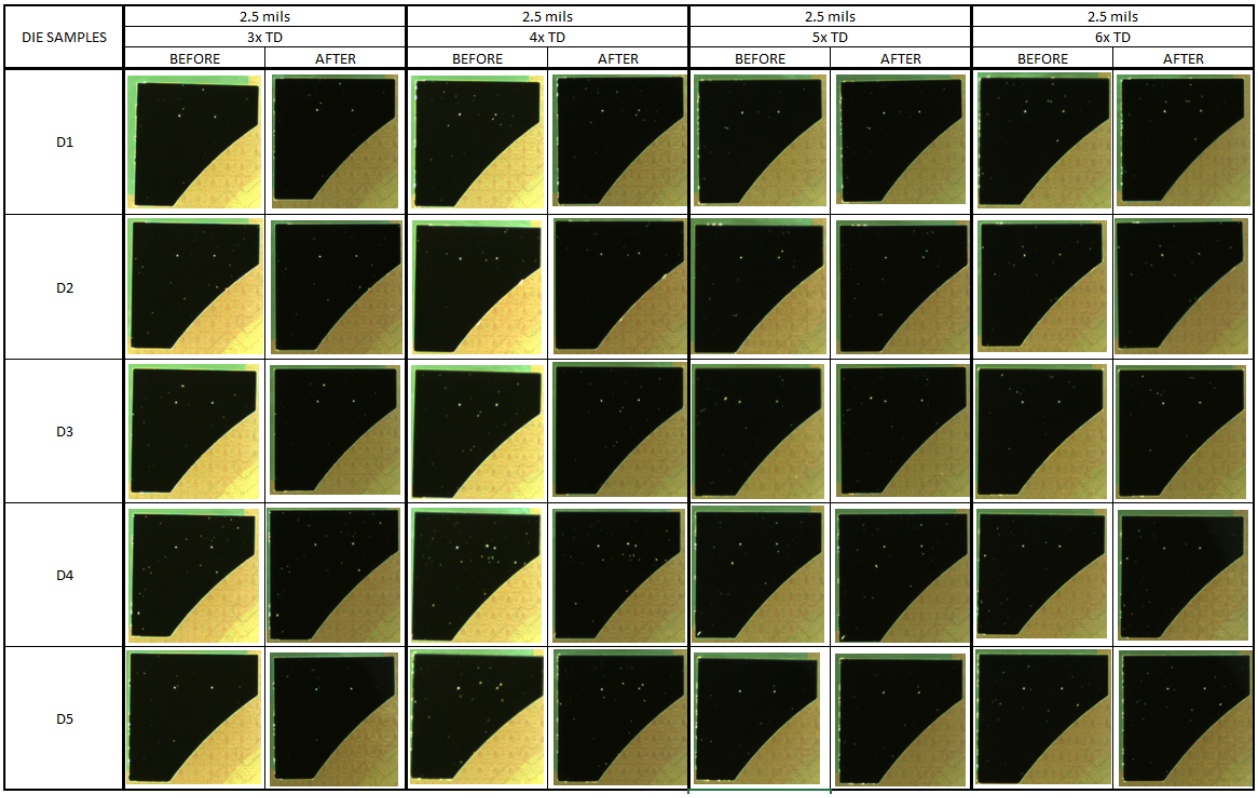
Appendix – D: Control Map of 240 Sampling Dice applicable for Product A Recon

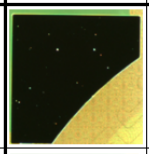
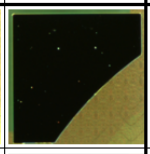
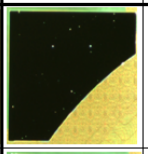
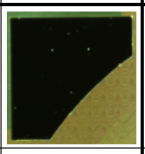
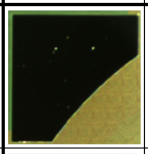
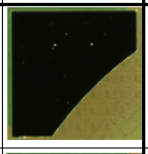
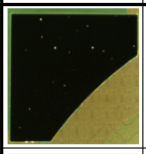
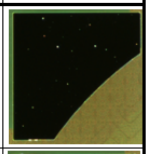
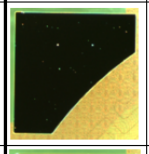
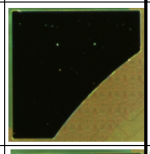
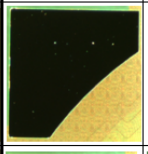
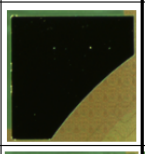
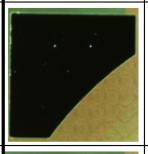
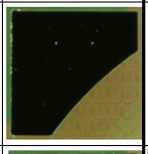
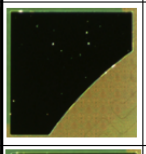
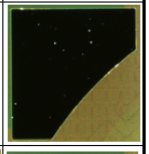
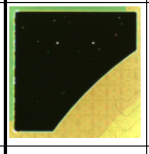
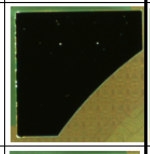
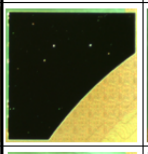
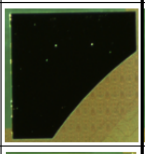
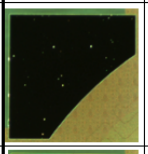
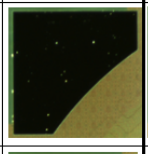
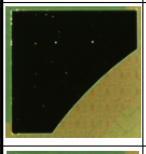
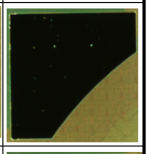
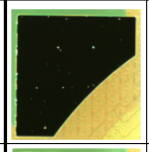
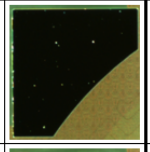
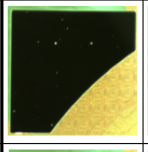
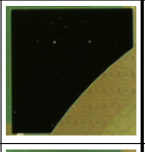
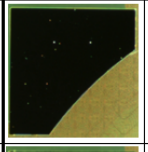
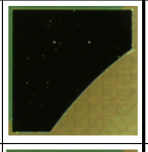
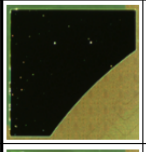
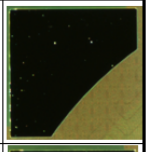
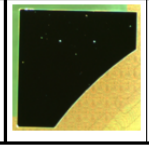
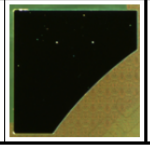
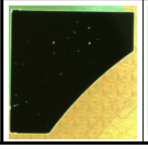
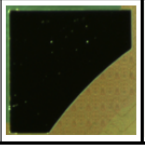
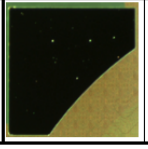
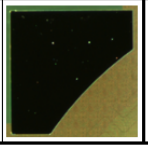
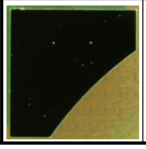
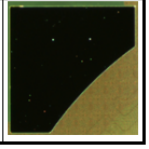


Appendix – E: Sampled dice used in 4 distinct sets with 10 dice per area



Appendix – F: Probing Process Capability Check



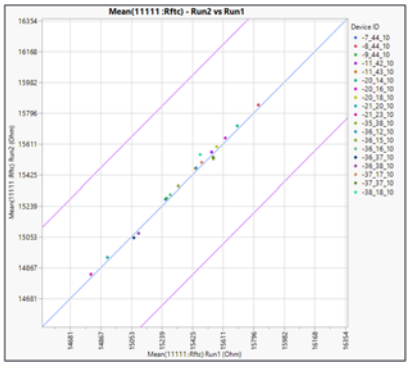
DIE SAMPLES	2.5 mils 3x TD		2.5 mils 4x TD		2.5 mils 5x TD		2.5 mils 6x TD	
	BEFORE	AFTER	BEFORE	AFTER	BEFORE	AFTER	BEFORE	AFTER
D6								
D7								
D8								
D9								
D10								

Appendix – G: Loop Run Test correlation in Machine 3 and Machine 1

Appendix – H: GRR Test Result per Test Parameter

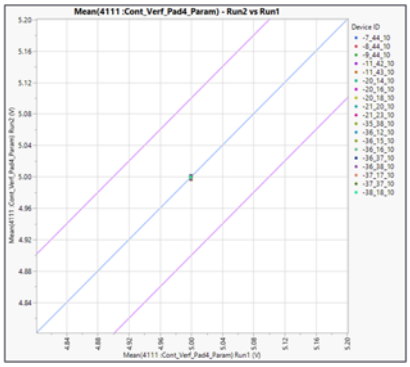
TEST_PARAMETER	GRR_LIMIT	Run1_grrStd	Run1_grrStd*3	GRR Result_grrStd	GRR Result_grrStd*3
3111 :Cont_Verf_Pad3_Param	0.1	0.001407	0.004220	0.001327	0.003980
4111 :Cont_Verf_Pad4_Param	0.1	0.001389	0.004167	0.001348	0.004045
4112 :Cont_Verf_MP1_Param_5V	0.1	0.000296	0.000889	0.000314	0.000943
4113 :Cont_Verf_MP2_Param	0.1	0.000314	0.000943	0.000253	0.000760
4114 :Cont_Verf_MP1_Param_2V	0.1	0.000310	0.000931	0.000221	0.000662
10121 :Info_Shunt_Current	2	0.006979	0.020938	0.007557	0.022672
11111 :Rftc	600	0.751369	2.254107	0.565685	1.697056
14111 :Info_MP1_V1	0.06	0.000295	0.000886	0.000181	0.000543
14112 :Info_PShunt_V3	0.002	0.000233	0.000700	0.000101	0.000303
15111 :Info_MP2_V2	0.002	0.000234	0.000703	0.000092	0.000277

Rftc GRR Result



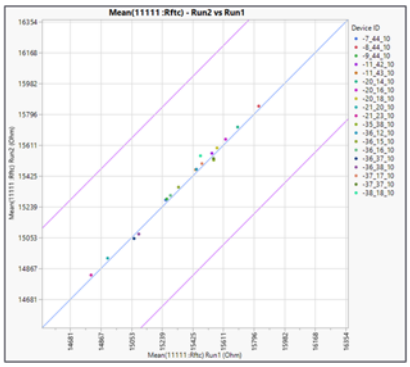
STATION ID	GRR Result
GRR RESULT	PASS
GRR ERR MAX	12.7%
GRR ERR MIN	-5.2%
GROUP AVG	15395.6742 (2.4%)
Nb samples	19
GRR Std Dev	3
GRR Limit	600
LSL	12000
USL	18000

Cont_Verf_Pad4_Param GRR Result



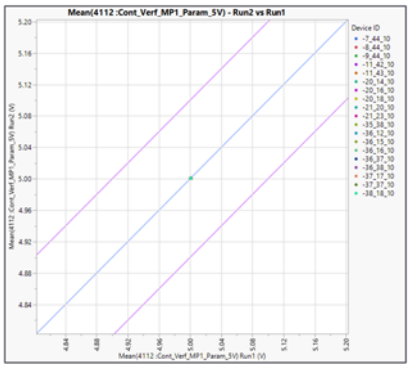
STATION ID	GRR Result
GRR RESULT	PASS
GRR ERR MAX	4.0%
GRR ERR MIN	-4.1%
GROUP AVG	4.998598 (0.0%)
Nb samples	19
GRR Std Dev	3
GRR Limit	0.1
LSL	4.5
USL	5.5

Cont_Verf_Pad3_Param GRR Result



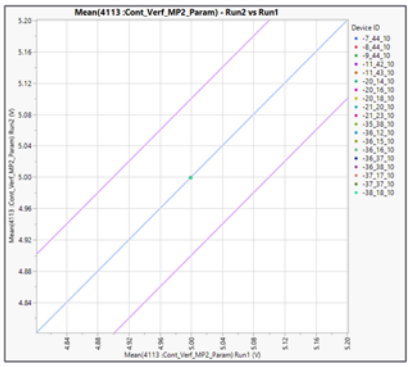
STATION ID	GRR Result
GRR RESULT	PASS
GRR ERR MAX	4.3%
GRR ERR MIN	-3.9%
GROUP AVG	4.998811 (0.1%)
Nb samples	19
GRR Std Dev	3
GRR Limit	0.1
LSL	4.5
USL	5.5

Cont_Verf_MP1_Param_5V GRR Result



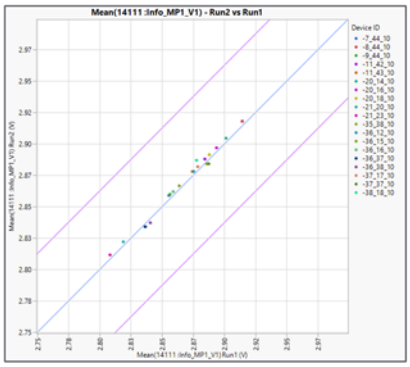
STATION ID	GRR Result
GRR RESULT	PASS
GRR ERR MAX	0.8%
GRR ERR MIN	-1.1%
GROUP AVG	5.001516 (0.0%)
Nb samples	19
GRR Std Dev	3
GRR Limit	0.1
LSL	4.5
USL	5.5

Cont_Verf_MP2_Param GRR Result



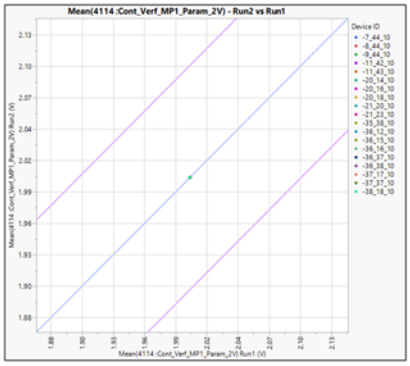
STATION ID	GRR Result
GRR RESULT	PASS
GRR ERR MAX	0.8%
GRR ERR MIN	-0.9%
GROUP AVG	4.998609 (-0.1%)
Nb samples	19
GRR Std Dev	3
GRR Limit	0.1
LSL	4.5
USL	5.5

Info_MP1_V1 GRR Result



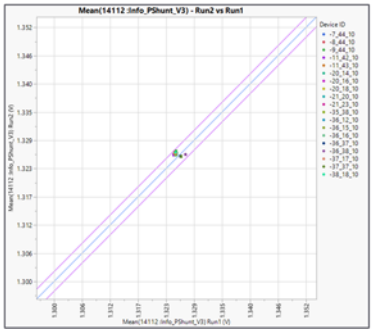
STATION ID	GRR Result
GRR RESULT	PASS
GRR ERR MAX	15.8%
GRR ERR MIN	-5.7%
GROUP AVG	2.870017 (4.0%)
Nb samples	19
GRR Std Dev	3
GRR Limit	0.06
LSL	2.2
USL	2.8

Cont_Verf_MP1_Param_2V GRR Result



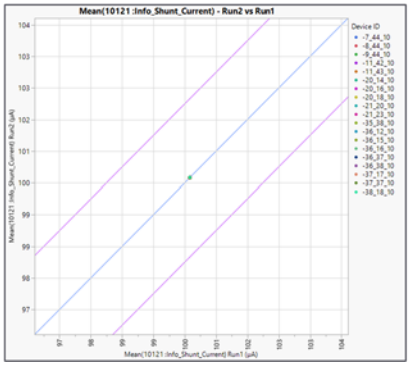
STATION ID	GRR Result
GRR RESULT	PASS
GRR ERR MAX	0.7%
GRR ERR MIN	-0.7%
GROUP AVG	2.001336 (-0.0%)
Nb samples	19
GRR Std Dev	3
GRR Limit	0.1
LSL	1.5
USL	2.5

Info_PShunt_V3 GRR Result



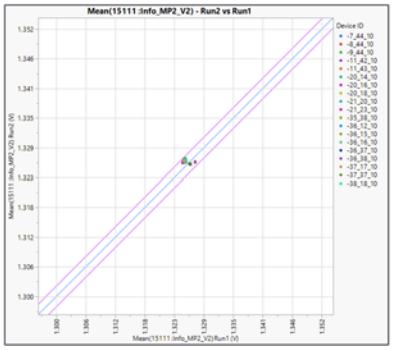
STATION ID	GRR Result
GRR RESULT	PASS
GRR ERR MAX	89.4%
GRR ERR MIN	-64.7%
GROUP AVG	1.326166 (43.9%)
Nb samples	19
GRR Std Dev	3
GRR Limit	0.002
LSL	0.99
USL	1.01

Info_Shunt_Current GRR Result



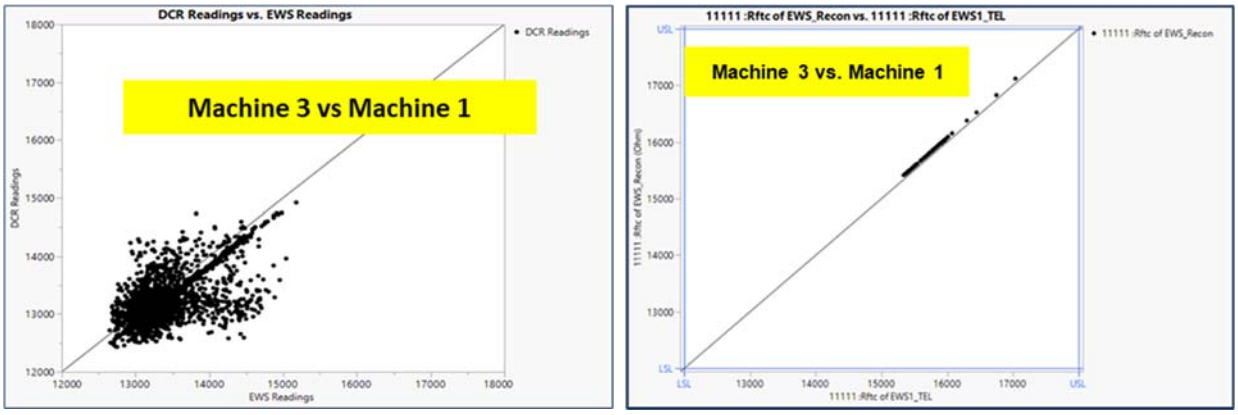
STATION ID	GRR Result
GRR RESULT	PASS
GRR ERR MAX	1.9%
GRR ERR MIN	-1.4%
GROUP AVG	100.260005 (0.2%)
Nb samples	19
GRR Std Dev	3
GRR Limit	2
LSL	90
USL	110

Info_MP2_V2 GRR Result



STATION ID	GRR Result
GRR RESULT	PASS
GRR ERR MAX	89.8%
GRR ERR MIN	-64.0%
GROUP AVG	1.326448 (44.3%)
Nb samples	19
GRR Std Dev	3
GRR Limit	0.002
LSL	0.99
USL	1.01

Appendix – I: Manual DCR vs Machine 1 Correlation

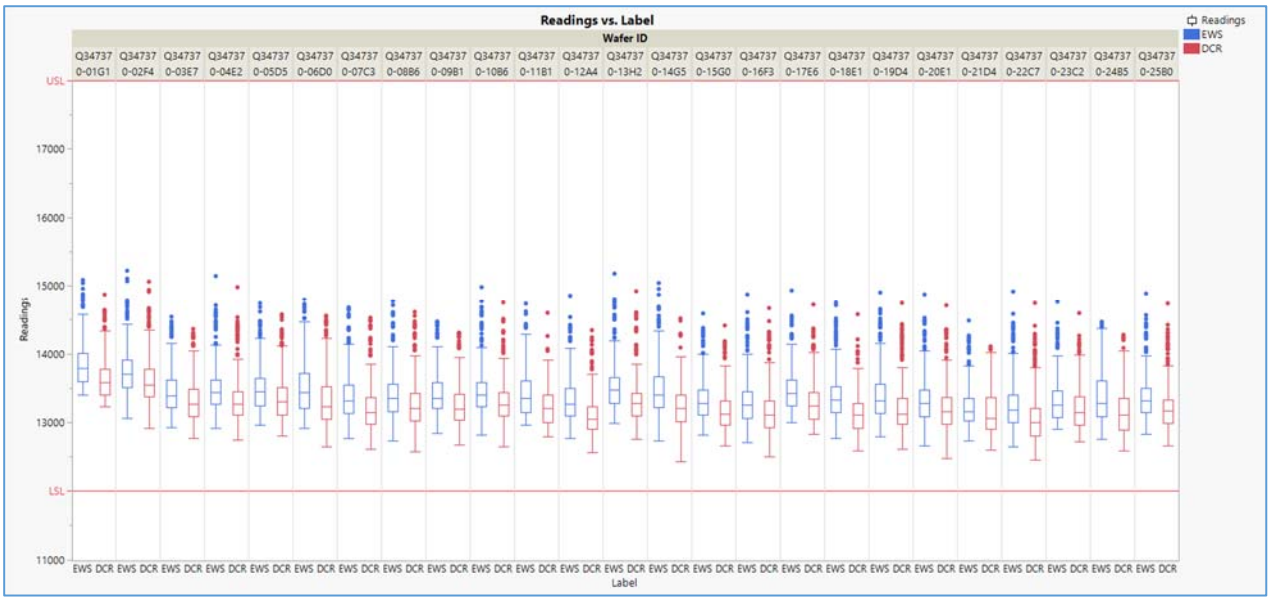


Appendix – J: Time Study Comparison between Full Test Auto DCR and Sampling DCR Test

			Full test			Sampling	240.00	
DCR TEST (8inch) EG			**Lot qty 31,972**	**Wafer Qty 3,442**	**# of wafers 1**	**Lot qty 31,972**	**Wafer Qty 3,442**	**# of wafers 1**
ITEM	**ELEMENT DESCRIPTION**	**freq**	**Average time per process element**	**Average SEC/UNIT**	**Remarks**	**Average time per process element**	**Average SEC/UNIT**	**Remarks**
1	Load cassette and search for wafers	lot	35.04	0.00110		35.04	0.00110	
2	Map view edit	lot	43.85	0.00137		43.85	0.00137	
3	Load recipe	lot	10.51	0.00033		10.51	0.00033	
4	Load program	lot	42.62	0.00133		42.62	0.00133	
5	Alignment	wafer	772.64	0.22447		772.64	0.22447	
6	Locating first die	wafer	63.25	0.01838		63.25	0.01838	
7	Test	wafer	25562.25	0.79952		191.88	0.05575	
8	Save map	wafer	36.56	0.01062		36.56	0.01062	
9	Index wafer out	lot	34.03	0.00106		34.03	0.00106	
10	Unload cassette	lot	12.31	0.00039		12.31	0.00039	
			Total Time (Sec/unit)	**1.05857**		**Total Time (Sec/unit)**	**0.31480**	
			UPH	**3,401**		**UPH**	**11,436**	
			DLC/day	**72**		**DLC/day**	**242**	
			Lots/day	**9.01**		**Lots/day**	**30.28**	
			Volume	**60**		**Volume**	**60**	
			No. of Wafer (12in)	**7.5**		**No. of Wafer (12in)**	**7.5**	
			No. of lot (Recon)	**17.4**		**No. of lot (Recon)**	**17.4**	
			No. of lots	**2**		**No. of lots**	**2**	
			Test qty	**63.944**		**Test qty**	**0.48**	
			Tester requirement	**0.89**		**Tester requirement**	**0.0020**	

Appendix – K: DCR Test Result

Lot	Wafer ID	Process	No of Samples	Pass Qty	Yield
784027JW01	Q347370-24B5	DCR	200	200	100.00%
784027JW01	Q347370-25B0	DCR	200	200	100.00%
784027JW02	Q347370-20E1	DCR	200	200	100.00%
784027JW02	Q347370-21D4	DCR	200	200	100.00%
784027JW02	Q347370-22C7	DCR	200	200	100.00%
784027JW02	Q347370-23C2	DCR	200	200	100.00%
784027JW03	Q347370-15G0	DCR	200	200	100.00%
784027JW03	Q347370-16F3	DCR	200	200	100.00%
784027JW03	Q347370-17E6	DCR	200	200	100.00%
784027JW04	Q347370-10B6	DCR	200	200	100.00%
784027JW04	Q347370-11B1	DCR	200	200	100.00%
784027JW04	Q347370-13H2	DCR	200	200	100.00%
784027JW04	Q347370-14G5	DCR	200	200	100.00%
784027JW05	Q347370-01G1	DCR	308	200	100.00%
784027JW05	Q347370-12A4	DCR	200	200	100.00%
784027JW05	Q347370-18E1	DCR	200	200	100.00%
784027JW05	Q347370-19D4	DCR	200	200	100.00%
784027JW06	Q347370-06D0	DCR	200	200	100.00%
784027JW06	Q347370-07C3	DCR	200	200	100.00%
784027JW06	Q347370-08B6	DCR	200	200	100.00%
784027JW06	Q347370-09B1	DCR	200	200	100.00%
784027JW07	Q347370-02F4	DCR	200	200	100.00%
784027JW07	Q347370-03E7	DCR	200	200	100.00%
784027JW07	Q347370-04E2	DCR	200	200	100.00%
784027JW07	Q347370-05D5	DCR	200	200	100.00%



Appendix – L: RFTC reading between the Auto DCR and Manual DCR Testing