EMBARKING AN INTEGRAL YIELD OPTIMIZATION JOURNEY THROUGH TECHNICAL RESEARCH UNCOVERING INNOVATION AND OPPORTUNITIES AT MIT WAFER RECONSTRUCTION PROCESS

Joseph C. Suarez
Reinadd Jan B. Abad
Judioz M. Manejero

WT & TNF Process Engineering – B2F2 Operations
STMicroelectronics Incorporated
#9 Mt. Drive, LISP2, Brgy. La Mesa, Calamba City, Laguna 4027
joseph.suarez@st.com, reinaddjan.abad@st.com, jude.manejero@st.com

ABSTRACT

One of the leading advances today is the fast-growing market for “superb technological devices”, enabling the evolution of industry towards smarter, safer, and more efficient factories & workplaces. At STMicroelectronics, we are keen to enhance this technological advancement specifically in module technology. A module is a distinct assembly of components that can be easily added, removed or replaced in a larger system. As new modules were introduced in back-end manufacturing, challenges lead to making everyday things smarter and connected.

The Optical Diffuser (ODIFF) line encompasses wafer mounting, sawing, and the wafer reconstruction process, with automated optical inspection at every critical step. A key station is the Wafer Reconstruction Process, which transfers wafer modules from 12-inch mounted tape to 8-inch, including inspections at the input, backside, and output stages. A thorough understanding of this new process is necessary to align with our customer’s expectations and identify service improvements. The new product's more complex design compared to legacy devices presents fresh challenges.

Addressing this challenge requires significant teamwork to ensure customer satisfaction, as this is the first instance of our production processing reconstructed wafers. During qualification, machine capabilities and limitations were carefully considered. The primary obstacle encountered was a high failure rate caused by Foreign Material (FM) on the die, detected by the optical system, which significantly impacted yield, machine efficiency, and line capacity. The primary objective is to restore yield and quality before starting mass production. New methodologies and designs have been proposed to address these issues and improve yield and capacity.

To address these challenges, it's crucial to understand that while FMs are inherent in cleanroom environments, they are manageable. Long-term improvement strategies are devised for control. The defects are mobile and can be eliminated. The team aims to eradicate these defects through design enhancements in new machinery. Process mapping revealed that FMs predominantly originate from environmental exposure, manual handling, material transport, and changes in operational procedures—specifically, a shift in fail logic from AND to OR. Additionally, machine-related issues such as difficulty in picking up dies, chipping, and scratches contribute to rejects.

Various proposals were developed from established design data to enhance processes, all subject to customer review, approval, and ongoing monitoring. Initiatives included cleaning peripherals, using a dedicated nitrogen cabinet for the reconstruction process, employing enclosed pushcarts, scanning wafers with a fan-type ionizer, installing air sweepers and new tools, and improving vision methods for indent detection. Comprehensive cleanroom training covered contamination sources and hazard control. Additional machine-specific yield issues were addressed with targeted improvements. These measures successfully reduced cosmetic defects and foreign material on dies, leading to quality enhancements in the Wafer reconstruction process and a notable yield increase.

1. 0 INTRODUCTION

Wafer reconstruction is a pivotal procedure in semiconductor manufacturing. It pertains to the process of rearranging functional chips on sticky tape affixed to a wafer ring post the sawing phase. The essence is to transform standard 12-inch wafers into sizes like 8, 6, 5, or 4 inches, or even reorganize chips based on specific features or grades.

1.1 MIT Optimus MR3 Machine

This machine is designed for use as an automatic die transfer machine for 8-inch and 12-inch wafer film frames. It is able to pick the singulated die from a populated, mapped and sawed wafer. Selected bin category from this input frame is placed into the output frame of pre-selected pattern which are all defined early in the recipe. A Vision Systems are installed on top of Input & Output wafer tables and Theta Inspection Station. Input camera and Output camera are used for die verification, inspection of surface defects and aid the wafer until die level alignment. Theta Vision is used for orientation inspection. Identification of the wafer ID, lot information and mapping request by using a Bar Code Scanner at Input Wafer Handler is also available shown in Fig. 1 and machine specification is shown on Table 1.

Fig. 1 Optimus MR3 Die Sorter Wafer to Wafer

Table 1: Optimus MR3 Specification

MACHINE PERFORMANCE SPECIFICATION	
Performance Specification	-Wafer-to-Wafer (Pick and Place) -Inspection (Top and Bottom)
Input Wafer	12 inches
Output Wafer	8 inches
Die Size	0.5x0.5mm to 15x15mm
Max Device Weight	5 grams
Placement Accuracy	+/- 30µm

It's well established that FM in a semiconductor manufacturing process can result in significant unplanned tool downtime, reduced product yields, and potential reliability issues. In the manufacturing industry, FM contamination is inevitable. It occurs in every facility at one time or another, but identifying and removing FM is vital to a manufacturer's success. When contamination goes undetected, it poses a potential danger to both the company and the consumer. The company risks losing consumer trust and damaging its brand reputation. Detection instruments should not be solely relied upon to prevent foreign objects but rather as the last line of defense in an integrated approach to preventing foreign object contamination from reaching the supply chain. Detection devices must be relevant to the contaminants that may be present in both the product and the process. Typical detection instruments most frequently seen in industries are Automated Optical Inspection (AOI) machines. They can provide additional data points and every finding should be logged, and a root-cause analysis performed to prevent future issues.

FM defined in this project are non-conductive fiber-like particles affecting mainly on semiconductor packages inviting such foreign materials to accumulate on the surface of the module. These foreign materials may cause quality issues on our costumer and worst on the end-user. See Fig. 2 for foreign material examples.

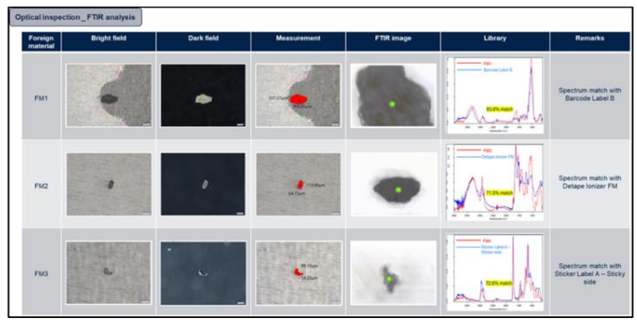


Fig. 2 Example of FM found on module

With process mapping, team have gain an overview of how foreign materials are carried out, how they can be improved or controlled, and how many steps are necessary to drive the process to its endpoint. Validation of defect contribution showed staging at N2 cabinet, Defect logic, Input Ionizer Bar, in between station and transport contributes increase on FM as shown in Fig. 3. And the graphical representation shown in appendix A.

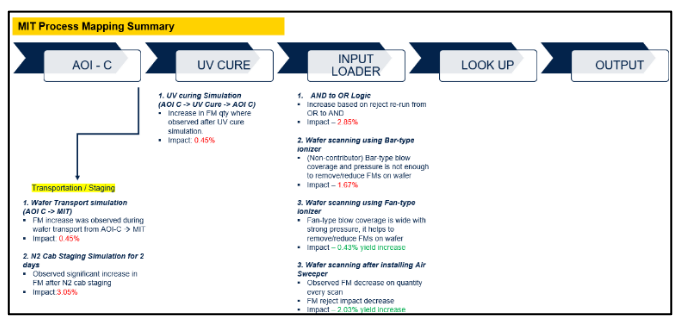


Fig. 3 Process mapping of FM

The objective of this project is to rally the overall process yield performance of Product A & Product B via improving foreign material failure rate, thereby refining quality performance in parallel through enhancement actions at Wafer Reconstruction process.

1.2 Foreign Material 5S Improvement

The 5S methodology is a powerful tool for optimizing operations. It's interesting to note how these principles, originating from Japan, have been widely adopted across various industries globally. By implementing 5S, organizations can indeed create a more organized, efficient, and safe work environment. This not only improves productivity but also enhances employee morale.

Prior L3 Build, the FM taskforce focused on improvement to critical stations identified. Focused on FM as the top yield loss contributor, the team performed different Design of Experiments (DOE). The purpose of DOE is to further understand its source and secondly is the formulation of steps or procedure on how to tackle the problem. Activities were performed to replicate the source of FM contamination. With this, the team formulation steps identified could be used to standardize team formulation practice. Several common FM improvements were performed to help increase the yield performance.

1.2.1 Wafer Staging and Washing

Staging and washing foreign material is a process often related to manufacturing. It involves preparing products for further processing and washing by removing contaminants, impurities, or any foreign matter. The team performed different DOE's at Saw washing to simulate and formulate steps to remove the FM.

1.2.2 Enclosed Push Carts

Enclosed pushcarts as shown in Fig. 4, are a type of material handling equipment designed to transport goods within a facility while providing a protective enclosure which offers great advantages when dealing with FM. In study, Enclosed pushcarts minimize the exposure of product to the environment, reducing the risk of FM contamination. They also help prevent cross-contamination between different materials or products. Using enclosed pushcarts can enhance the perception of a facility's commitment to quality and professionalism. In conclusion, the use of enclosed pushcarts for transporting can significantly contribute to maintaining quality, safety, and efficiency, while also supporting compliance with industry standards and regulations.

Fig. 4 Enclosed Push Cart

1.2.3 Dedicated N2 Cabinets

Dedicated nitrogen cabinets, also known as dry boxes or desiccator cabinets, are storage solutions designed to maintain a controlled atmosphere, typically a low-humidity environment for the storage and handling of moisture-sensitive materials. It is essential in maintaining the integrity of moisture and oxygen-sensitive materials during production. Proper usage and maintenance of these cabinets are crucial for their effective operation. The control of foreign materials is crucial to ensure product quality and safety. Regular inspection is implemented to check for any foreign materials in the N2 including visual inspections and the use of Particle Count tool to detect any foreign objects. Refer to Fig. 5.

Fig. 5 Particle Count tool

1.3 Input Ionizer Sweeper

FM sweeper on input wafer is composed of 1 Bar type static eliminator and a controller. The controller is made up of VK332V-5G-M5 solenoid valve, Omron H3DK-M2 timer relay, Banner 1033H optical sensor, Festo LRMA-QS-4 pressure regulator, ISE40A-01-R pressure sensor, G2R-1-SND relay and connecting wires.

The aim of this equipment improvement is to remove these defects by introducing machine design enhancement to the new machine. The change performed is via installing sweeper on input loader railway to remove mobile FM on input wafer. To optimize the effectiveness of input ionizer sweeper, validations were performed to know the optimum setting of Air flow pressure. To assess the removal effectivity, during DOE's, foreign material particle was intentionally placed on wafers before validation and observing the performance after running with the sweeper installed.

1.4 Indents of Inspection Region

The inspection region can be further modified based on the indents set by product design requirement. The indents can have either positive or negative values, i.e., the inspection region will be reduced or enlarged respectively. Indents can be set separately for each inspection region in this module set. One possible use of indents is to avoid immediate regions around the package boundaries where surface intensities very often are non-homogenous due to chamfer surfaces.

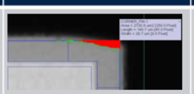
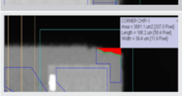
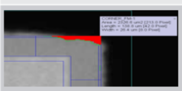
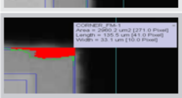
1.4.1 Change Indent from 15um to 30um ROI for Corner FM

Because of the change in fail logic of FM from AND to OR logic which is much tighter, high rejection rates due to false alarms is also one of the significant issues that the team encountered. False alarms can lead to wasted resources. To address this issue the team implemented strategies to reduce false alarms while maintaining a high level of accuracy by adjusting the threshold for triggering an alarm. This involves setting the threshold at a level that minimizes false alarms while still capturing genuine events. To address the FM false rejection, Region of Interest (ROI) indent was optimized.

1.4.2 Change Indent from 15um to 30um ROI for Chipping

Following the Indent change in corner FM, the team address the over rejection on chippings by making necessary adjustments to the inspection parameters. Potential impact on the results were considered after adjusting the indent for the ROI in a chipping. A preliminary test was performed and results from previous data were used as comparison as shown in Table 2.

Table 2. False alarm due to change in Fail Logic

Criteria	Sample Image	MIT Measurement	Remarks
Corner Chip: 1. Reject when L and W > 50 µm 2. Reject if any glass chipping reached to contact pad **Side Chip:** 1. Reject if W chipping > 50 µm. 2. Reject if L chipping > 2270 µm (measured by shifting 30 µm datum line) **Backside FM:** ø < 50 µm OR < 2000 µm2		Area= 2730.8 um² Length = 148.7 um Width = 29.7 um	Chippings Logic = Pass Corner FM Logic = Fail
		Area= 3681.1um² Length = 186.2 um Width = 39.4 um	Chippings Logic = Fail
		Area= 2326.6 um² Length = 138.8 um Width = 26.4 um	Chippings Logic = Pass Corner FM Logic = Fail
		Area= 2075.4 um² Length = 152.0 um Width = 19.8 um	Chippings Logic = Pass Corner FM Logic = Fail
		Area= 2960.2 um² Length = 135.5 um Width = 33.1 um	Chippings Logic = Pass Corner FM Logic = Fail

1.5 Installation of Suck and Blow

The primary cause for not reaching the desired yield in the wafer reconstruction process is the rejection of input wafers due to the presence of FM. Despite ongoing improvements, the yield target has not yet been achieved. And with highest contributor of FM related rejects on input wafer inspection.

To further reduce and improve Input FM Reject, the team implement a suction and expulsion system designed to dislodge and eliminate mobile foreign materials before the inspection stage. Suck and blow assembly consists of static eliminator, pressure regulator, vacuum sensor and vacuum cup. It is located on opposite side of the wafer table to suck every foreign material that been blown away by the static eliminator as shown in Fig. 6.

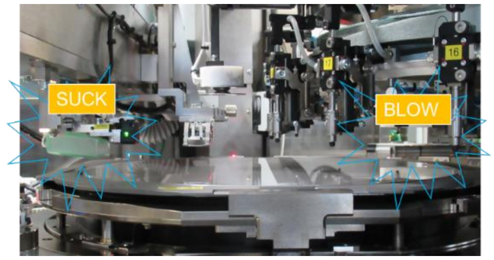


Fig. 6 Installed suck and blow at input wafer table.

1.6 Hard to Pick Die

The longer the die are on tape, the more they adhere. Even if the tape is chosen for its low adhesive level over time, at some point it will be difficult to remove the die. At Wafer Reconstruction process, if the die is not picked correctly on the mounted tape, it is referred to as a Hard to pick die. This issue arises due to the stickiness of the mounted tape itself and due to Collet/Pick Up tool having a vacuum issue or an ejector needle that is out of alignment during pickup. Fig. 7 shows the wafer with hard to pick die.

Fig. 7 Wafer with Hard to pick die

2. 0 REVIEW OF RELATED WORK

Prior studies on foreign material reduction have focused on various strategies and technologies to minimize contamination and improve product quality. Such studies include the use of high-precision sensors to detect foreign materials in real-time, Material Handling Improvements, Process Optimization, and Designing and testing mechanical systems to physically remove contaminants.

The findings from previous studies provide valuable insights into effective strategies for foreign material reduction. They serve as a foundation for developing and implementing improved contamination control measures and serves as the motivation for this study.

3.0 METHODOLOGY

3.1 Wafer Staging and Washing

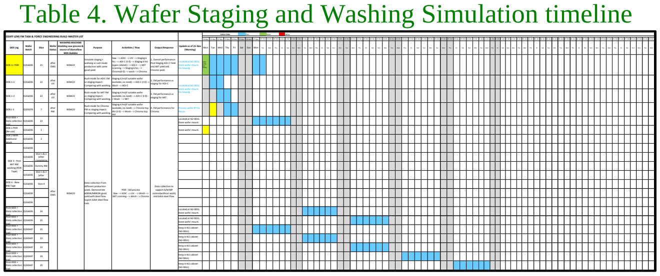
3.1.1 Wafer Staging and Washing Simulation and DOE

DOE was performed for the wafer staging and washing simulation. This comprises of 6 legs following different condition of staging and washing as shown on Table 3. For this simulation, each leg uses 1 12'' wafer approximately 7900 units. Following the Qualification timeline on Table 4, the idea is to well manage the data collection by rigorously following the ideal flow task timeline.

Table 3. Wafer Staging and Washing Simulation table

DOE Leg	Description	Objective	Time Interval	A	B	C	D	E			F			G			H		
				[illegible]	[illegible]	[illegible]	SAW	AOIC	WASH	STAGING	UV	WASH	STAGING	MIT	WASH	STAGING	CHROMA	WASH	STAGING
1+ POR	POR flow with additional staging without any wash	Simulate staging + washing vs rush mode production with the same good yield. Send sample of FM for FA Analysis	T-0	✓	✓	✓	✓	✓	N/A	E	✓	N/A	E→E						
			T-1	N/A	N/A	N/A	N/A	✓	N/A	E→E									
			T-2	N/A	N/A	N/A	N/A	✓	N/A	N/A	N/A	N/A	N/A	✓	✓	N/A	✓	N/A	E→H
			T-2'	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	✓	✓→H	
			T-3	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	✓→	END	
1 - 1	Rush mode for AOI-C FM vs staging vs wash	Data collection on FM differences using AOIC. Send sample of FM for FA Analysis	T-0	✓	✓	✓	✓	✓	N/A	N/A	✓	N/A	E→E						
			T-1	N/A	N/A	N/A	N/A	✓	✓→E										
			T-2	N/A	N/A	N/A	N/A	✓→	END										
1 - 2	Rush mode for MIT FM vs staging impact vs wash	Data collection on FM differences using MIT. Send sample of FM for FA Analysis	T-0	✓	✓	✓	✓	✓	N/A	N/A	✓	N/A	E→E						
			T-1	N/A	N/A	N/A	N/A	✓	✓	N/A	N/A	N/A	N/A	✓→	END				
1 - 3	Rush mode for Chroma FM vs staging impact vs wash	Data collection on FM differences using Chroma. Send sample of FM for FA Analysis	T-0	From staged remnant (2 weeks)													✓	✓→H	
			T-1	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	✓	✓→H	
			T-2	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	✓→	END	
POST DOE+ ADDIR	FM mapping under POR flow using Addir wafer	Data collection from different production week. Demonstrate ADDIR/MERON good yield with ideal flow.	T-0	✓	✓	✓	✓	✓	N/A	N/A	✓	N/A	N/A	✓	N/A	N/A	✓→	END	
POST DOE+ MERON	FM mapping under POR flow using Meron wafer		T-0	✓	✓	✓	✓	✓	N/A	N/A	✓	N/A	N/A	✓	N/A	N/A	✓→	END	

Table 4. Wafer Staging and Washing Simulation timeline



3.2 Input Ionizer Sweeper and installation of suck and blow

3.2.1 Input Ionizer sweeper and installation of suck and blow Validation

Team drive is the observed spike on the input FM defects at MIT during PRB (Production Build) run. With this, improvement in terms of FM reduction were done on the MIT Input assembly setup to address the issue gearing up towards PVT (Production Validation Test) build milestone. The foreign material that been swept by the static eliminator will directly push towards the suction holes as shown in Fig. 8. The design is composed of a static eliminator that serve as sweeper and been triggered by the optical sensor with 10 secs delay time allotted to fully sweep the whole wafer.

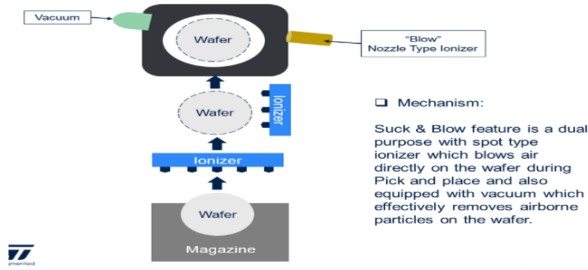


Fig. 8 Detailed photo of every parts location

3.2.2 Validation of effectiveness procedure

Validating the effectiveness on the installed MIT improvement is a critical step to ensure that it meets the intended objectives and performs reliably. The validation process typically involves several procedures as shown on Table 5.

Table 5. Effectiveness validation procedure

1	Prior validation, measure the ESD and Ion Balance check (Offset voltage & Decay time) on the Suck & Blow.	
2	Inspect the 12'' wafer to be used for the validation. This will serve as the POR data.	
3	Record the After-scan yield, Reject impact %.	
4	Record the Parameters / Condition used:	
	4.1	ESD and Ion Balance
	4.2	Air sweeper condition
	4.3	Fan type Ionizer
	4.4	Load Frame Speed
	4.5	Sweeper Pressure Condition
	4.6	Record the Result

3.3 Foreign Material Mapping

To further validate the FM defects detected at MIT, need to submit multiple samples to FA for FTIR/SEM EDX analysis to understand the potential FM sources as shown on Table 6. The objective is to complete the mapping per critical process, station source materials and conduct FA based on actual reject samples gathered at MIT step to have a continuous improvement and to aid and complement our yield bridge for further FM rejection improvement

Table 6. Wafer Staging and Washing Simulation timeline

Device:	ADDIR-PVT		MERON-PVT	
Lot No:	784027JW03	784027JW07	78402X902	78402X901
Wafer Batch:	Q347370	Q347370	Q345512	Q345512
Slices #:	15,16,17	2,3,4,5	5,6,7,8	1,2,3,4
FA Request:	CLB-IMD_24_00070	CLB - IMD_24_00083	CLB-IMD_24_00073	CLB-IMD_24_00077
	CLB-IMD_24_00071	CLB - IMD_24_00084	CLB-IMD_24_00074	CLB-IMD_24_00078
	CLB-IMD_24_00072	CLB - IMD_24_00085	CLB-IMD_24_00075	CLB-IMD_24_00079
		CLB - IMD_24_00086	CLB-IMD_24_00076	CLB-IMD_24_00080

3.4 Indents of Inspection Region

When adjusting the indent from 15µm to 30µm for the ROI, it is important to consider the potential impact on the results through careful validation and documentation.

3.4.1 Indents of Inspection Region procedure

The procedure for inspecting indents in a specific region, is a meticulous process that ensures the integrity and quality of products. Table 7 shows the step-by-step guide to conducting an inspection for indents.

Table 7. Indents of Inspection Region procedure

1	Adjust the equipment settings by navigating to the control panel of the indentation equipment.
2	Use a standard sample to perform a preliminary test with the new indent.
3	Compare the results with previous data to understand the changes.
4	Conduct several tests to ensure consistency in the results.
5	Continuously monitor the results.

3.5 Hard to Pick die (HTP)

When dealing with a "hard to pick" issue, a Design of Experiments (DOE) approach can be valuable for identifying the critical process parameters. The DOE methodology allows for systematic variation of input variables to understand their impact on the output, in this case, the difficulty of picking a particular item.

3.5.1 MIT Process Parameter DOE for Hard to pick issue

Table 8 presents the machine parameters that were identified. Each leg of the DOE was conducted. Key parameters for the MIT related to HTP, including Eject Up Height, Eject Up Speed, Pick Dwell, Pick Force, and Wafer Tape Press Down (Input), were recorded. A sample size of 100 units was utilized for each leg of the DOE. Additionally, the HTP failure rate was collected for the analysis.

Table 8. MIT machine settings DOE

DOE	Condition	Eject up Height	Eject up Speed	Pick Dwell	Pick Force	Wafer Tape Press Down (Input)
		0.49 0.55 mm	60 80%	50 100 ms	90 120 gf	3 to 5 mm
1	OOS Ejector Height	0.40	80	80	110	-5
2	OOS Ejector Height	0.40	60	100	110	-5
3	OOS Ejector Height	0.40	60	80	100	-5
4	OOS Ejector Height	0.40	80	90	120	-5
5	OOS Ejector Height	0.40	80	80	120	5
6	OOS Ejector Height	0.40	70	90	120	-5
7	OOS Ejector Height	0.40	60	100	110	-5
8	OOS Ejector Height	0.40	70	100	100	-5
9	OOS Ejector Height	0.40	70	90	100	-5
10	OOS Ejector Height	0.40	80	80	100	5
11	OOS Ejector Height	0.40	60	90	120	-5
12	OOS Ejector Height	0.40	70	100	110	-5
13		0.50	60	90	120	-5
14		0.50	80	90	100	-5
15		0.50	70	80	110	5
16		0.50	60	90	110	-5
17	POR Setting	0.50	70	100	120	-5
18		0.50	70	80	110	-5
19	Max Setting (Speed/Dwell/Force)	0.50	80	100	120	-5
20		0.50	60	80	120	-5
21		0.50	70	90	100	-5
22		0.50	60	80	110	5
23		0.50	80	100	100	-5
24		0.50	80	100	100	-5
25		0.55	60	90	100	5
26		0.55	70	90	110	-5
27		0.55	80	90	110	-5
28		0.55	70	100	120	-5
29		0.55	80	100	110	-5
30		0.55	60	100	120	-5
31		0.55	70	80	100	-5
32		0.55	60	100	100	-5
33		0.55	80	90	110	-5
34		0.55	80	80	120	-5
35		0.55	70	80	120	-5
36	Min Setting (Speed/Dwell/Force)	0.55	60	80	100	-5
37	OOS Wafer Expansion Table using POR	0.50	70	100	120	-6

3.5.2 UV Dosage/Intensity DOE

For UV dosage DOE, Both DOE 1 and DOE 2 were performed as seen in Table 9, each with a different Speed Setting. It's essential to measure the actual UV exposure dose at the UV machine during these experiments. Additionally, the process should be carried out at MIT 2, and completed one round of RW with 3.2k units for each leg of the DOE. Following these steps, thus obtained the HTP failure rate.

Table 9. MIT machine settings DOE

DOE Plan	POR	DOE 1 1RW – 3442 units	DOE 2 1RW – 3442 units
Speed	20mm/sec	15mm/sec	10mm/sec
Exposure Dose	92.8 mJ/cm2	133.0 mJ/cm2	199.7 mJ/cm2
Maximum Intensity	42.84 mW/cm2	45.28 mW/cm2	44.98 mW/cm2

4.0 RESULTS AND DISCUSSION

4.1 Wafer Staging and Washing Simulation and DOE Interpretation and next plan.

Based on the data provided, AOI-C consistently shows high yields, with the lowest reported at >98.80%. Post-DOE adjustments have led to an improvement, with yields reaching up to 99.60%. Foreign Material (FM) is a significant factor affecting yield, particularly at the MIT stage, where the yield dropped to 88.46%. The Chroma process appears to be stable, with yields generally above 95%. The highest yield reported post adjustments is 97.0%. Both the Product A & Product B adjustments post-DOE have resulted in improved yields compared to the DOE 1+ POR baseline. Refer also at table 10 for summary and interpretation.

Table 10. Wafer Staging and Washing Simulation and DOE

DOE Leg	Description	Objective	Summary and Interpretation	Key take-aways	Next Plan
1+ POR	POR flow with additional staging without any wash	Simulate staging + washing vs rush mode production with the same good yield. Send sample of FM for FA Analysis	• Three AOI-C runs having >99% yield on average with a yield loss of 0.80%. • MIT shows a drop in yield due to FM • The leading detractor at second Chroma is Bin 16, accounting for 4.83% of all rejections – with additional staging waiting for Chroma Availability. • Major contributor of yield loss are at MIT and CHROMA with 89.90% and 95.60% yield respectively.	• The outcome demonstrates that staging has no discernible impact on FM buildup. • The Back-side inspection in Chroma may also be impacted by staging in dead bug wafer recon.	• Continuation of DOE with the introduction of wash as cleaning method of mobile FM. • Send sample dice of Bin 76 rejects at AOI-C for FA using remnants of Wafer Q316035-21 Addr. • Send sample dice of Bin 16 rejects at AOI-C for FA using remnants of Wafer Q316035-21 Addr.
1 - 1	Rush mode for AOI-C FM vs staging vs wash	Data collection on FM differences using AOIC. Send sample of FM for FA Analysis	• Three runs of AOI-C are performed, along with extra staging and washing. • FM contribution was increased by 0.96% on average, resulting in an overall yield of >99.0% at AOI-C.	• The findings indicate that while staging had no discernible impact on FM buildup, washing after 2nd AOI-C has increased the amount of FM. • Cleaning the sawn wafer using the washing method (beneath and with the die surrounding) is not useful in removing mobile FM.	• Continuation of DOE with the introduction of wash as a cleaning method of mobile FM at MIT.
1 - 2	Rush mode for MIT FM vs staging impact vs wash	Data collection on FM differences using MIT. Send sample of FM for FA Analysis	• Two AOI-C runs having >98.80% yield on average however build up of FM after wash was observed causing 2nd AOI-C to fall at 1.79% yield loss. • The yield drops to 88.46% overall at MIT.	• Concerning washing at DOE 1 – 1, Mobile FM cannot be removed from the sawn wafer by cleaning it with the washing procedure (below and with the die surrounding).	• Continuation of DOE with the introduction of wash for mobile FM at CHROMA • Send sample dice of Bin 38 rejects at MIT for FA using remnants of Wafer Q316035-22 Addr. • Installation of 2nd Air (Ionizer) sweeper to remove dust, saw debris, and other contaminants from the die surfaces.
1 - 3	Rush mode for Chroma FM vs staging impact vs wash	Data collection on FM differences using Chroma. Send sample of FM for FA Analysis	• Two runs of Chroma are performed, with washing in between each cycle. • Wafer remnant subject had already been staged for two weeks. • 95.58% was the overall Chroma yield recorded.	• Even after weeks of staging, there is still no appreciable difference in FM accumulation. • Staging in dead bug wafer recon affected the Back-side inspection in Chroma with the same condition as DOE 1+ POR. • Cleaning the sawn wafer using the washing method (beneath and with the die surrounding) is not useful in removing mobile FM.	• Continuation of DOE using POR flow for Addir and Meron without staging and wash. • Send sample dice of Bin 16 rejects at AOI-C for FA using remnants of Wafer Q325074-07 Addr.
POST DOE+ ADDIR	FM mapping under POR flow using Addir wafer	Data collection from different production week. Demonstrate ADDIR/MERON good yield with Ideal flow.	• Overall yield for AOI-C was 99.60%, with a 0.40% impact of FM Reject • A comparable result of yield was observed. 96.17% versus 89.80% (on DOE 1+ POR) with a delta of 6.30% yield. • The Chroma resulted in 97.0% yield overall.	• Noticeable that 2nd recon has the highest count of FM out of 3 recon wafers at MIT with an overall 2.97% yield loss. • Looking in-depth and MIT's design of picking (vertical serpentine path), as the wafer expands during picking, the dust bursts and releases as FM into the surrounding area, or worse, the entire wafer surface. • Turret rotation significantly impacts 2nd Wafer recon. 2nd MIT-PNP is near the revolving turret causing an air sway inside the machine. As this air sways constantly, FM flows and spreads around the wafer surface.	• Replication of POST DOE + ADDIR using MERON to check for the commonality of response.
POST DOE+ MERON	FM mapping under POR flow using Meron wafer	Data collection from different production week. Demonstrate ADDIR/MERON good yield with Ideal flow.	• Replication of Post DOE + using Meron wafer under POR flow. • Overall yield for AOI-C was 99.0%, with a 0.91% impact of FM Reject. • A comparable result of yield was observed. 95.76% versus 89.80% (on DOE 1+ POR) with a delta of 6.0% yield.	• Still, noticeable that 2nd recon has the highest count of 3 recon wafers at MIT with an overall 4.10% yield loss. • Same response with Addir wafer, air sways inside the machine causing saw dust and other debris to spread.	• Optimizing the Picking method at MIT input. • Upgrade of Blow and Suck at MIT input. • Introduction of Air sweeper at the output assembly of MIT and Input of CHROMA.

4.2 Input Ionizer Sweeper installation of suck and blow

4.2.1 Input Ionizer Sweeper validation result

Overall, the project brought 60% reduction of foreign material on wafer surface. Foreign material reject drops down to 1.36% during CT build and 1.4% during PRB build. There was a yield improvement of 4.7% for Product A during the engineering wafer evaluation run compared to the PRB run, with yields increasing from 93.28% to 97.98%. Additionally, observed a 0.98% yield improvement at the Input station in terms of FM reduction during the evaluation run versus the PRB Build. The ESD measurements and Ion Balance checks, which include Offset voltage and Decay time, for the Suck & Blow station passed successfully. There was no significant difference in the measurements during the PRB and pre-PVT runs for both Product A & Product B. Regarding Die pick-up stability, no die exceeded a 1.5-degree rotation that would necessitate realignment at the aligner. As seen in Fig. 13. Also see appendices B1 to B4 for other validation results.

4.2.2 Suck and Blow validation result

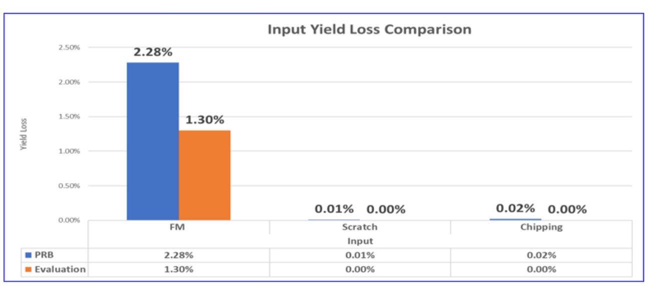


Fig. 13 Input Yield Loss

4.3 FM Mapping FA Result

The FA results of PVT from the top FM contributors shown on Table 11 and 12, which were derived from MIT Recon remnants, indicate the following: The top contributor, with a 95.00% share, is Elemental Peaks, with potential sources being Metal Cassette and wafer frame. The second highest contributor is Bulk Label / Barcode Label from a 2-in-1 Labeler, accounting for 8.00%. Lastly, the Face Mask is identified as the third contributor, making up 2.00% of the total.

With the result of the FM analysis, the team have generated a separate Quality campaign on these FM sources across the productions line. On top of this, Main contributor is due to Cassette/Frame debris hence have established a cleaning procedure of the Jigs/Fixtures on daily basis with monitoring.

Table 11. Product A FA Result Summary

Lot ID:	Batch:	Wafer Slice#:	e-WIP:	FA Report:	Sample Photo:	Result:
784027JW03	Q347370	15	CLB-IMD_24_00070	Microsoft Edge PDF Document		[illegible]
784027JW03	Q347370	16	CLB-IMD_24_00071	Microsoft Edge PDF Document		[illegible]
784027JW03	Q347370	17	CLB-IMD_24_00072	Microsoft Edge PDF Document		[illegible]
784027JW07	Q347370	2	CLB - IMD_24_00083	Microsoft Edge PDF Document		[illegible]
784027JW07	Q347370	3	CLB - IMD_24_00084	Microsoft Edge PDF Document		[illegible]
784027JW07	Q347370	4	CLB - IMD_24_00085	Microsoft Edge PDF Document		[illegible]
784027JW07	Q347370	5	CLB - IMD_24_00086			[illegible]

Table 12. Product B FA Result Summary

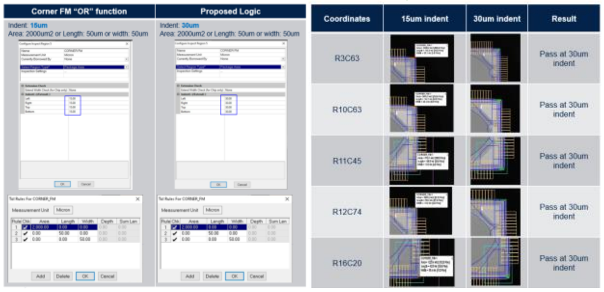
Lot ID:	Batch:	Wafer Slice#:	e-WIP:	FA Report:	Sample Photo:	Result:
78402X902	Q345512	5	CLB-IMD_24_00073	Microsoft Edge PDF Document		[illegible]
78402X902	Q345512	6	CLB-IMD_24_00074	Microsoft Edge PDF Document		[illegible]
78402X902	Q345512	7	CLB-IMD_24_00075	Microsoft Edge PDF Document		[illegible]
78402X902	Q345512	8	CLB-IMD_24_00076	Microsoft Edge PDF Document		[illegible]
78402X901	Q345512	1	CLB-IMD_24_00077	Microsoft Edge PDF Document		[illegible]
78402X901	Q345512	2	CLB-IMD_24_00078	Microsoft Edge PDF Document		[illegible]
78402X901	Q345512	3	CLB-IMD_24_00079	Microsoft Edge PDF Document		[illegible]
78402X901	Q345512	4	CLB-IMD_24_00080			[illegible]

4.4 Indents of Inspection Region validation results

4.4.1 Change Indent from 15um to 30um ROI for Corner FM

As a result, Failed units which passes the corner chippings criteria passed at 30um indent. Most of the FM call out were categorized as Good as seen in Table. 13.

Table 13. Result after the adjustment



4.4.2 Change Indent from 15um to 30um ROI for Chippings

After changing the indent from 15um to 30 um ROI for chippings, as seen in Table 14, an initial gain of 26.57% reduction on the misdetection of Corner chipping (Backside). Also, 0.77% Yield recovery from the 2.90% fallout due to Corner Backside chipping with this proposal. Also refer to the Appendices C1 and C2 for the other validation done.

Table 14. Summary of Indent from 15um to 30um

	Wafer #	15um indent	30um indent	% reduce
# of Chippings	Q315052-01	134	131	2.24%
	Q315052-02	224	163	27.23%
	Q315052-03	378	184	51.32%
	Q315052-04	187	133	28.88%
	Q315052-05	151	116	23.18%
			Average	**26.57%**

4.5 Hard to Pick die DOE Result

4.5.1 MIT Process Parameter DOE for Hard to pick

Based on the DOE results, several key conclusions can be drawn regarding factors influencing high-temperature probe (HTP) fails. Firstly, a lower Eject up height appears advantageous, with an out-of-spec (OOS) threshold identified at 0.4mm. Secondly, a slower Eject up Speed correlates with fewer HTP fails. Thirdly, a higher Pick Dwell Time, particularly at a slower rate, is associated with better performance in minimizing HTP fails. Additionally, maintaining Pick Force at 100gf demonstrates optimal performance. Furthermore, the analysis indicates that setting Wafer expansion at -6mm results in higher HTP fails compared to the standard POR settings at -5mm as shown in Fig. 14 and Table 15.

Considering these findings and the Prediction profiler, the optimal combination of parameters to reduce HTP rejects entails a configuration that aligns with the following guidelines established from the DOE results: a low Eject up height, slower Eject up Speed, higher Pick Dwell Time, and a Pick Force of 100gf. Additionally, it suggests maintaining the Wafer expansion setting at the standard POR level of -5mm to mitigate HTP fails effectively as shown in Table 16. Also see appendices D1 and D2 for the parameter DOE result.

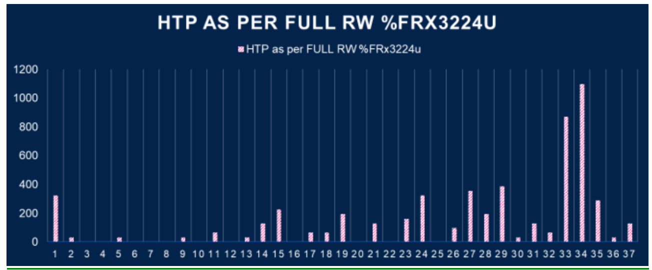


Fig. 14 HTP DOE Result

Table 15. MIT Parameter Overall Summary

Zero Failure rate combinations

Eject up Height	Eject up Speed	Pick Dwell	Pick Force	Wafer Tape Press Down (Input)	%FR	HTP as per FULL RW	Prediction on Profiler
0.4	60	80	100	-5	0	0	402
0.4	80	90	120	-5	0	0	281
0.4	70	90	120	-5	0	0	155
0.4	60	100	110	-5	0	0	198
0.4	70	100	100	-5	0	0	91
0.4	80	80	100	-5	0	0	370
0.4	70	100	110	-5	0	0	39
0.5	60	90	110	-5	0	0	289
0.5	60	80	120	-5	0	0	375
0.5	60	80	110	-5	0	0	351
0.55	60	90	100	-5	0	0	341

Table 16. MIT Optimized Parameter Setting

EJECT UP HEIGHT	EJECT UP SPEED	PICK DWELL	PICK FORCE	WAFER TAPE PRESS DOWN (INPUT)
0.4	70	100	100	-5
0.4	70	100	110	-5

4.5.2 UV Dosage/Intensity DOE to eliminate Hard to pick issue validation result

Table 17 shows that operating at a slower speed can lead to a reduction in occurrences of hard to pick and a lower overall failure rate. However, it's important to balance speed with efficiency and productivity to find the optimal operating conditions for any given system. See Appendix E for the UV External Measurement.

Table 17. UV Parameter DOE result

DOE Plan	POR	DOE 1 1RW – 3442 units	DOE 2 1RW – 3442 units
Speed	20mm/sec	15mm/sec	10mm/sec
Exposure Dose	92.8 mJ/cm2	133.0 mJ/cm2	199.7 mJ/cm2
Maximum Intensity	42.84 mW/cm2	45.28 mW/cm2	44.98 mW/cm2
Result	**64 units Hard to pick**	**52 units Hard to pick**	**19 units Hard to pick**
Failure Rate	**2.41%**	**1.51%**	**0.55%**

4.6. Overall Summary and Results

To tackle top detractors by WK07, namely FM Input and Hard to Pick, additional MIT improvements have been put into action. As a result of these efforts, the overall Wafer Reconstruction Yield has shown a significant improvement, surging from 89% to an impressive 99%. As shown in Fig. 15. Also see appendices F1 to F4 for the yield and result per product.

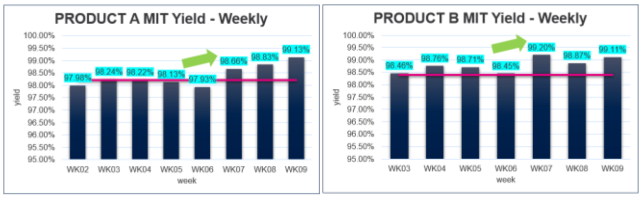


Figure 15. Product A & Product B Weekly Yield summary

5.0 CONCLUSION

Based on the findings, the presence of foreign materials from the environment contributed significantly to the overall impact accounting for 3.05%. Additionally, manual handling and transportation of materials such as using push carts, had a notable impact of 0.45%. The change in fail logic from AND to OR logic had a substantial impact of 2.85%. Furthermore, the defects investigation revealed that wafers were staged on an engineering cabinet with various materials, including papers, labels, and shipper boxes, while other rejects were attributed to machine-related issues such as "Hard to Pick," "Chipping," and "Scratching."

In conclusion, the combination of environmental foreign materials, manual handling, recipe logic changes, and staging issues has contributed to the overall impact on the process. Addressing these factors will be crucial in mitigating the impact of foreign materials and improving the quality of the production process.

Consequently, the effectiveness of the formulated machine, material, method and environmental control solutions was validated during the qualification and engineering phases, where it was incorporated into the system and successfully addressed quality issues related to foreign material. By implementing these improvements at the beginning of the engineering milestone there were no quality issues observed.

As a result of these developments, the new tools, parameters, and methodology have been established and incorporated into the final stages of the reconstruction process for mass-production. The project's an integral yield optimization journey has been successful with the thorough technical research uncovering innovation and opportunities at MIT wafer reconstruction and has led to the manufacturability of the new product.

6.0 RECOMMENDATIONS

The present investigation represents a definitive solution by replacing manual handling with fully automated technology, effectively addressing specific manufacturing challenges. With the favorable outcomes of the study, operations can integrate this transition into the mass production of the latest device and extend its application to future devices with similar customer requirements.

7.0 ACKNOWLEDGMENT

The authors express their gratitude to the management of STMicroelectronics Calamba for consistently inspiring their technical staff to develop innovative solutions in the evolving technology landscape. The support of the Department sponsor and B2F2 Director, Ms. Aileen V. Gonzales for the support, and encouragement throughout the project. The entire team's backing, particularly from the Process Technician group, is also acknowledged. Furthermore, the Line Sustaining and Equipment Engineering group's contributions and cross-checks during the project's implementation phase are appreciated.

8.0 REFERENCES

1. **Foreign Material Removal through Optimization of Vacuum and Blow FM Kit** | Michael D. Capili. Back-End Manufacturing & Technology, STMicroelectronics, Inc.

2. **MIT Semiconductor Pte Ltd** | Vision Maunual, OM05A-20-1-R03

3. **4JM Solutions Wafer Reconstruction** https://4jmsolutions.com/equipment/semiconductor-sensor-discrete-components/front-end/wafer-reconstruction/

9.0 ABOUT THE AUTHORS

Joseph C. Suarez is currently a Test and Finish Senior Process Technician in STMicroelectronics since 2023 and is assigned at Odiff AOI Process Engineering department for Operations 2. He received his B.S Degree in Industrial Engineering from University of Perpetual Help system DALTA in Calamba, Laguna

Reinadd Jan B. Abad, is currently a Senior Test and Finish Process Engineer in STMicroelectronics and is assigned at Test and Finish department for Operations 2. He received his B.S Degree in Electronics and Communications Engineering from

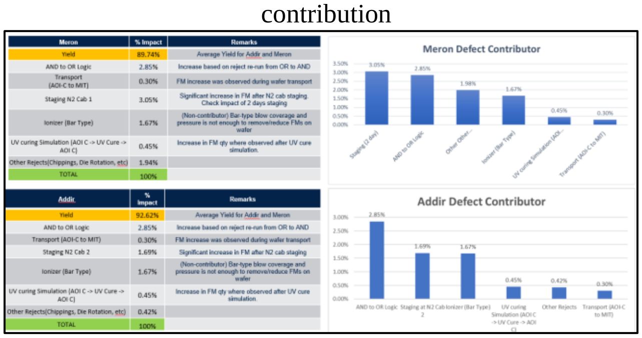
University of the Cordilleras in Baguio City.

Judioz M. Manejero is currently a Test Process Manager in STMicroelectronics and is managing Test and Finish department for Operations 2. He received his B.S Degree in Electronics and Communications Engineering from Mapua University in Intramuros, Manila.

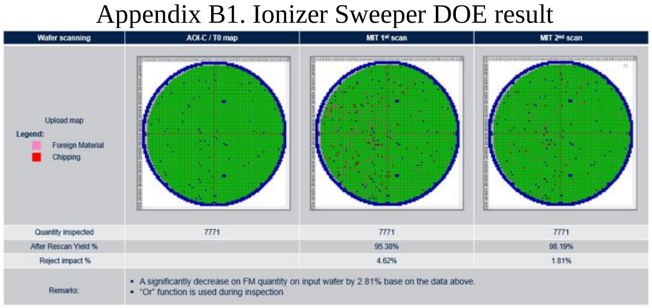
10.0 APPENDIX

This section includes figures and tables that are too bulky to be placed next to the discussion. It helps to maintain the smooth flow of discussion while maintaining the technical merit of the study through appropriate data and figures. Each appendix should be identified using an alphabet, with corresponding description (e.g., Appendix A – Cumulative Standard Normal Distribution Constants).

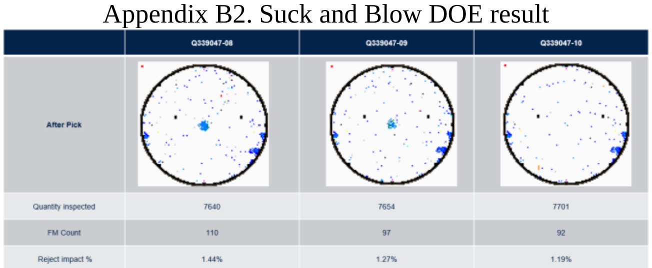
Appendix A: Graphical representation of the defect's contribution



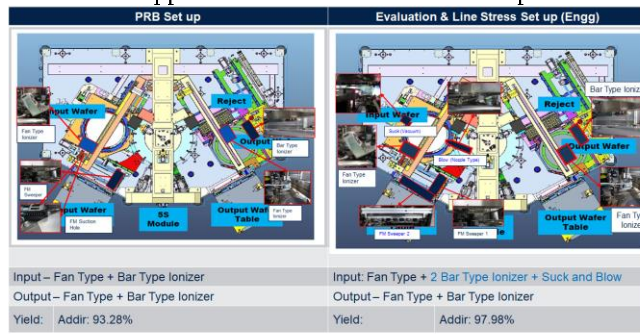
Appendix B1. Ionizer Sweeper DOE result



Appendix B2. Suck and Blow DOE result



Appendix B3. Suck and Blow Set-up

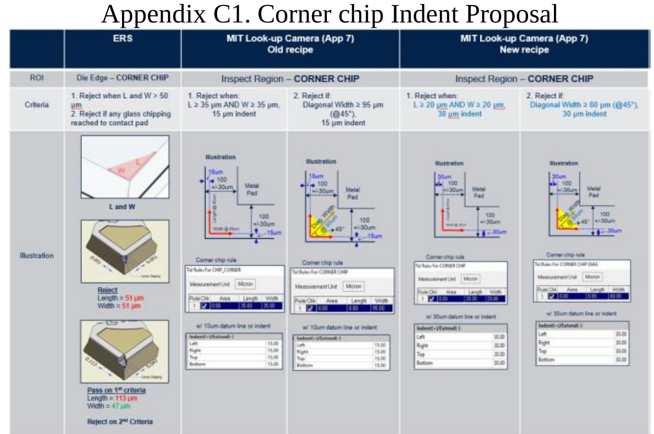


Appendix B4. ESD Check of Ionizer

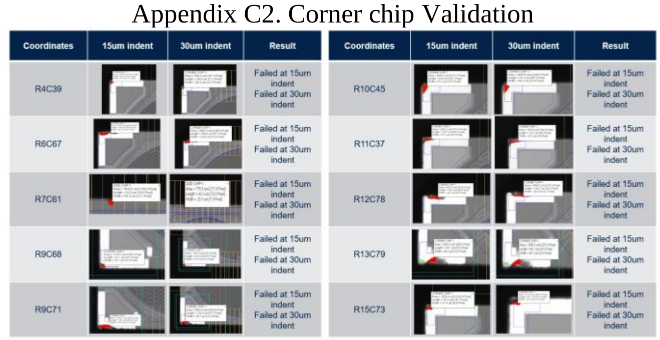
Description of Item Checked	Readings 1st	Readings 2nd	Readings 3rd	Remarks
Ion balance (V) Requirement : <±30V	-12 V	-9 V	-6 V	Passed
+ve Decay time (s): Requirement : <8s (Malibu Specs)	2.9 secs	2.1 secs	2.1 secs	Passed
-ve Decay time (s): Requirement : <8s (Malibu Specs)	2.7 secs	2.4 secs	1.8 secs	Passed

All parameters / conditions passed the ESD measurement.

Appendix C1. Corner chip Indent Proposal

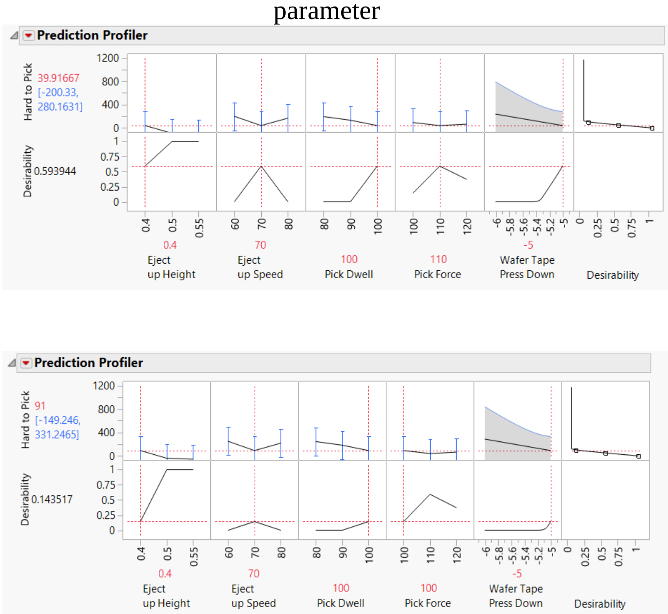


Appendix C2. Corner chip Validation

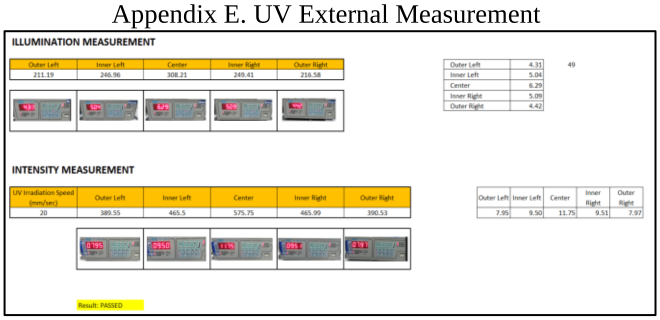


Appendix D1. HTP Parameter DOE Result

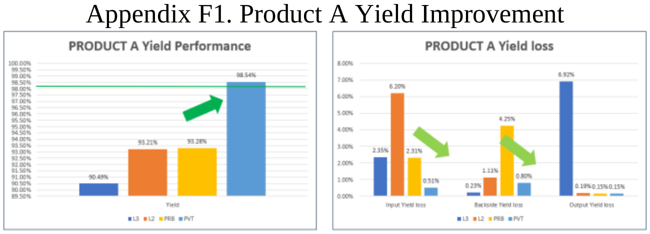
Appendix D2. Prediction Profiler of MIT Recommended parameter



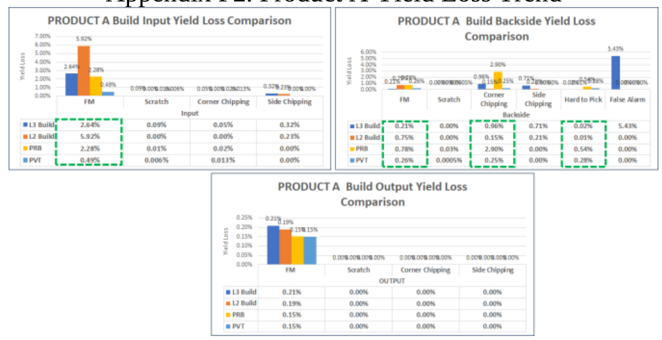
Appendix E. UV External Measurement



Appendix F1. Product A Yield Improvement



Appendix F2. Product A Yield Loss Trend

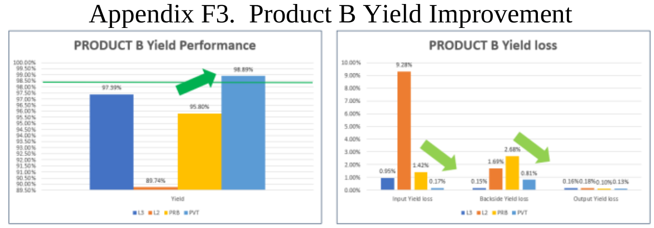


Product A Yield Result

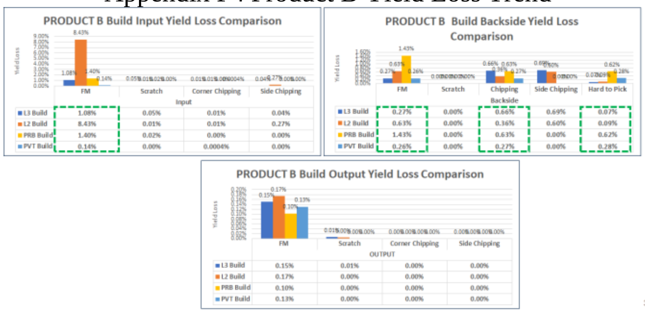
The current Product A PVT yield achieved during the MIT Recon process stands at 98.54%, meeting the target of 98.20%. There has been a remarkable improvement of 5.26% in Product A PVT yield compared to the PRB yield performance, escalating from 93.28% to 98.54%. Significant enhancements have been noted particularly in Input & Backside Yield loss during the PVT milestone. Various improvements have been implemented in the PVT MIT process, including enhancements like FM Sweepers, Suck & Blow, ROI 30um Indent, Blade Dressing, and FM Controls before MIT.

The total yield loss for Product A across Input, Uplook, and Output stations amounts to 1.46%. A notable improvement has been observed particularly at FM Input, Backside FM/chipping, and Hard to Pick stages during the PVT Milestone. Furthermore, a comparative assessment of performance at the Output station has been conducted in comparison to previous builds.

Appendix F3. Product B Yield Improvement



Appendix F4 Product B Yield Loss Trend



Product B Yield Result

The current Product B PVT yield achieved during the MIT Recon process stands at 98.89%, surpassing the target of 98.40%. Product B PVT yield has shown a notable increase of 3.09% compared to the PRB yield performance, rising from 95.80% to 98.89%. A significant enhancement has been observed in Input & Backside Yield loss during the PVT milestone. Various improvements have been implemented in the PVT MIT process, including enhancements like FM Sweepers, Suck & Blow, ROI 30um Indent, Blade Dressing, and FM Controls before MIT.

The Product B total yield loss amounts to 1.11% across Input, Uplook, and Output stations. There has been a notable improvement observed particularly at FM Input, Backside FM/chipping, and Hard to Pick stages during the PVT milestone. Additionally, a comparative analysis of performance at the Output station has been conducted in relation to previous builds.