Device "T" Electrical Yield Improvement

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ABSTRACT

One of the key metrices in semiconductor testing is yield as it determines both quality and productivity.

In this paper, DMAIC methodology (**D**efine, **M**easure, **A**nalyze, **I**mprove, **C**ontrol) was used in order to solve an electrical yield loss issue encountered during final testing of an als & proximity sensor module device *at ams OSRAM Group.,* where 1% loss is equivalent to thousands of dollars of loss for a one-year forecast. The device suffered yield loss due to proximity quasi trim and proximity noise failures which constitutes for 60% of the total failure pareto. During the analysis, factors were identified and were related to Machine *(shutter kit design limitation),* Method *(reference trim table)* and Material *(high vcsel power and low asic sensitivity).* The solutions implemented for Machine and Method had an impact of improved yield by 2.4%. On the other hand, the cause related to the VCSEL and ASIC materials *which were found to be within the fab process windows* are considered out-of-scope of the project and are suggested to be studied further for future products.

1. 0 INTRODUCTION

Final test is considered one of the last gate in semiconductor manufacturing and testing prior delivery of parts to customers. Here, yield loss issues on module level could mean several potential factors from Fab to Assembly and from Test process itself.

There is also a limitation on what can still be improved, specially for a mass production device, any redesign or specification changes for ASIC or Package will pose a huge impact requiring process change for the company and needing customer's approval. These cases are hence considered out-of-scope for this project.

1.1 Proximity Sensor Module

Basically, a proximity sensor module consists of an Infrared *(IR)* light source and IR photodiode as a detector. It provides object detection via the reflected IR light. An example is a mobile device to the screen user's ear.

In module, it is built with the ASIC, filters, Vcsel and packaged into a clear mold or enclosed with lid.

1.2 Test Setup and Test Program

Proximity sensors are trimmed and calibrated in the factory. The test setup and the test program plays a huge role on ensuring proper calibration of the units. The test setup must have good mechanisms to support the test for proper calibration which would need tests in dark and light positions, with and without *(proximity*) target and several others. The setup and the program must be in total sync to allow accurate measurements specially in timings and actuation of the peripherals during test.

1.3 Proximity Test Parameters

Several test parameters are necessary to ensure full functionality of devices. And for a proximity sensor the device needs to be calibrated where pre-trim measurements are taken to determine the offset needed to reach the desired target and later on trimmed. In such case, a quasi trim is necessary to find the best trim code possible prior actually fusing or trimming the parts.

Also the noise level is measured in order to assure the accuracy and consistency of proximity measurement.

There are more functional tests needed to ensure device functionality, but this paper will only cover relevant tests under study.

1.3.1 Proximity Quasi Trim

Proximity quasi trim is a measurement done to find the best trim code from a reference trim table to trim the proximity device to specified target.

1.3.2 Proximity Noise

Proximity noise test is measured as a coefficient of variation. It measures the variability of proximity values and reject parts with high variation which may cause issues on the user application.

2. 0 REVIEW OF RELATED WORK

Not Applicable.

3.0 METHODOLOGY

3.1 Define Phase

The goal of the project is to improve the electrical yield by at least 0.5% this is after consideration of the potential risks such as: valid fails with no potential recovery, accepted process (Fab, Assy) windows, and limitation on design or test capability.

This goal is aligned with relevant stakeholders and the team who will support the analysis and improvement.

3.2 Measure Phase

The process involved, it's current performance and data variability is visualized in order to identify the focus area as part of preparation for the analyze phase.

Fig.1 shows main process steps at final test and the focus process is on the electrical test.

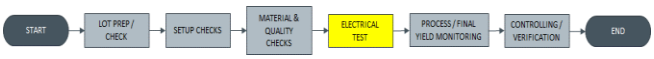

Fig.1. Process mapping for final test.

The current electrical yield performance of the device as shown on Fig.2 has an average of 96.5% and with low CPK at 0.21 only. Moreover, multiple lots fall below the target yield set for the device.

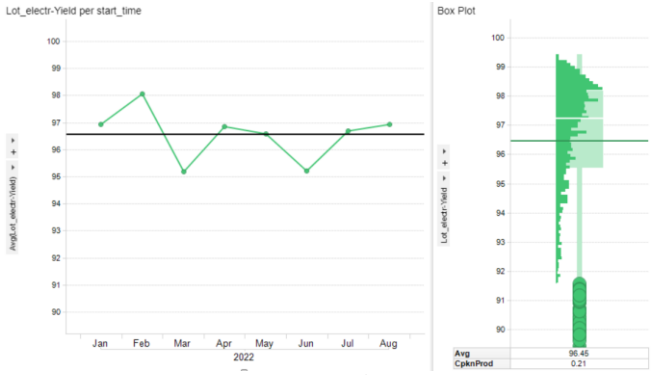

Fig.2. Showing the electrical yield trend of the device and the statistics indicating the average and CPK below the intended targets.

The failing parameters were put into a pareto chart to determine which failures should be focused. Fig.3 shows the top 2 failures observed which contributed to 60% of the overall fails. These are (1) proximity noise and (2) proximity quasi trim parameters

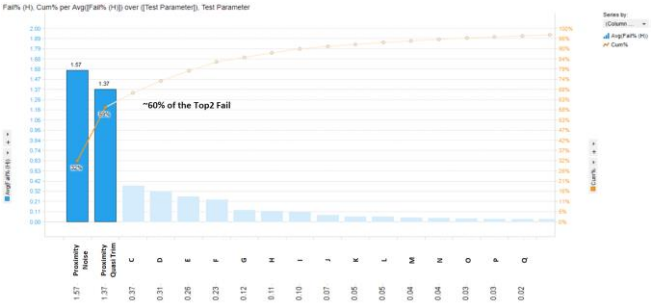

Fig.3. Showing the top 2 failing parameters that will be subjected for analysis

3.3 Analyze Phase

Ishikawa diagram as shown on Fig.4 was used to show all the potential factors along with the tabular assessment and ranking for prioritization as shown in Fig.5.

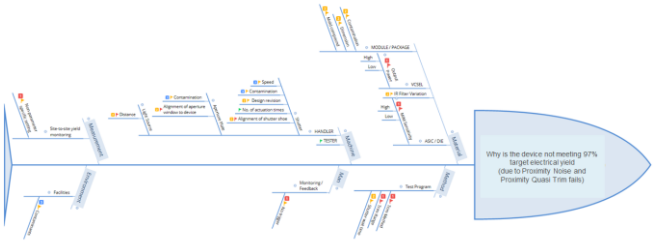

Fig.4. Ishikawa Diagram including Material, Machine, Method, Measurement, Man, Environment

Assessment of potential Root Causes

Category 6M1E	Working hypothesis X1, X2, ... Xn	Ranking Red/Yellow/Green or CNX	Evidence for ranking	Y1 Eyield / Lot	Y2 Prox_Cap_Gain_Quasi	Y3 Prox_Pulse_Noise	Priority for verification	Method applied for verification
Material	Low / High MIM Cap Sensitivity	Red	Test data results	9	9	9	1	FT and WAT Data correlation analysis
	Filter variation / anomaly	Yellow	Test data results	1	1	1	2	Parameter data correlation analysis and inspection
	Low / High VCSEL output power	Red	Test data results	9	9	3	1	FT and LIV Data correlation analysis
	Contaminations on module package	Yellow	Team input	9	3	9	2	Package inspection & defect experiment correlation
	Package dimension variation	Yellow	Team input	3	3	3	2	Package inspection
	Mold compound variation	Yellow	Team input	3	3	3	2	Package inspection
Machine	Shutter Shoe mis-alignment	Red	Expert Input	9	9	9	2	Test Setup Check & Verification
	High Shutter speed	Yellow	Team input	3	3	3	3	Test Setup Check & Verification
	Shutter Design Rev	Yellow	Team input	3	3	3	2	Data correlation Analysis
	Shutter actuation times	Green	Team input	1	1	1	-	TP revision check
	Aperture plate – window and device mis-alignment	Red	Expert Input	9	9	9	2	Test Setup Check & Verification
	Contaminations on shutter assy	Yellow	Expert Input	3	3	3	3	Test Setup Check & Verification
	Contaminations on aperture window	Yellow	Expert Input	3	3	3	3	Test Setup Check & Verification
	Light source distance	Red	Test data results	9	9	1	2	Test Setup Check & Verification
Method	Trim Method	Yellow	Data results	3	3	3	1	Data Analysis Trim Experiment
	Trim Range	Red	Data results	9	9	1	1	Data Analysis Trim Experiment
	Shutter control wait time	Yellow	Team input	3	3	3	2	Test Analysis old vs new wait time
Measurement	No specific parameter setup for Site-to-site Yield Monitoring	Yellow	Team input	1	1	1	2	Test Setup Check
Man	No trigger for test hold and feedback	Yellow	Team input	1	1	1	2	Test Setup & OCAP Check
Environment	Contaminants	Yellow	Team input	1	1	1	3	Test Setup Check

Fig.5. Assessment of potential root causes showing the ranking and expert's assessment

The potential factors were individually verified according to their ranking and prioritization and 20 factors were reduced to 4 potential factors.

Material

x_1 ASIC Low metal-in-metal (MIM) capacitance sensitivity caused by higher oxide thickness (within Fab process window).

x_2 VCSEL increased Output power (within Fab process window).

Machine

x_3 Shutter kit design

Method

x_4 Reference Trim table

Subsequent analysis shows the method and results of the validation for the 4 potential factors.

3.3.1 ASIC Low MIM Cap sensitivity

As shown in Figs.6-7 One of the potential factors found to have statistically significant relationship with the increased failure rate of both parameters mentioned *(Prox Quasi Trim & Prox Noise)* was a Fab parameter MIM capacitance. Interquartile1 of the MIM capacitance was used for the trend line to show that lots with lower values got higher failure rate on the mentioned tests.

Fig.6. MIM Capacitance Interquartile1 (Q1) and Prox Quasi Trim Fail rate (%) trend and regression analysis showing statistical significance. As the MIM capacitance value decreases the failure rate increases.

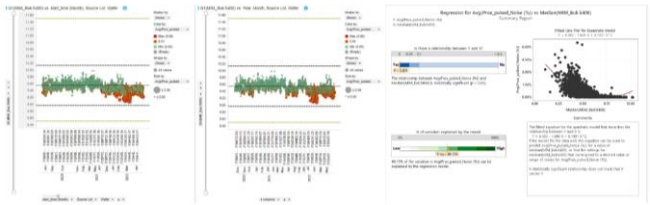

Fig.7. MIM Capacitance Interquartile1 (Q1) and Prox Noise Fail rate (%) trend and regression analysis showing statistical significance. As the MIM capacitance value decreases the failure rate increases.

3.3.2 VCSEL increased Output power

Another factor that showed statistically significant relationship with the yield loss encountered was the higher VCSEL output power (Po). Median (Q2) of the Vcsel output power was used to analyzed and correlate with the failure rate as shown in Fig.8

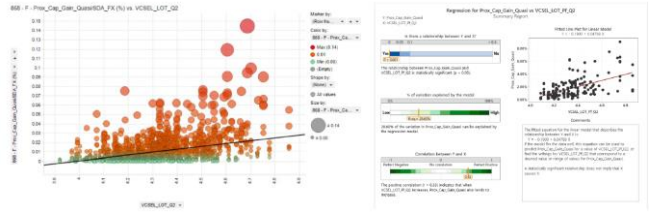

Fig.8. Vcsel Po median (Q2) and Prox Quasi trim fail rate (%) trend and regression analysis showing statistically significant relationship. As the Vcsel Po increases the failure rate of the Prox quasi trim also increases.

3.3.3 Shutter kit design (Setup)

The shutter kit is a mechanism that opens and closes the aperture to allow dark and light tests. Fig.9 shows an illustration of the shutter kit and their position.

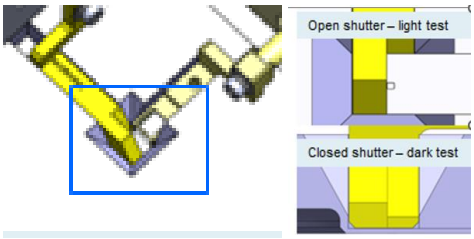

Fig.9 Aperture plate illustration with shutter kit mechanism that supports actuation to allow tests at light and dark.

Here the wait time control of the TP and the shutter speed of the setup must be in sync to allow accurate tests. With position of the shutter not affecting any measurements.

A split experiment was conducted to validate two factors.

(1) Setup shutter kit (Old, New)

(2) Test program (TP) shutter control wait time

Table.1 shows the split analysis conducted with old and new shutter kit and with different shutter control wait time for dark and light tests (60/60ms, 80/75ms, 100/90ms)

Sourcelot	Vcsel Lot	MainQty	Lot Split	Status	TP_ShutterControl	Setup / Shutter Kit	Test Quantity	Noise Fails	Noise %
Sourcelot A	VCSEL Lot A	27,839	Lot A	PS	Current	M49 _H (Old)	10344	116	1.14
			Lot B	PS	dark, light = 60, 60 ms	M29_L (New)	10079	63	0.63
			Lot A1	Exp	Mid	M49 _H (Old)	1236	20	1.64
			Lot B1	Exp	dark, light = 80, 75 ms	M29_L (New)	1241	15	1.21
			Lot A2	Exp	Previous	M49 _H (Old)	1242	16	1.3
			Lot B2	Exp	dark, light = 100, 90 ms	M29_L (New)	1241	10	0.81

Table.1 split analysis table for shutter kit and TP control wait time

Chi-Square % defective test was used to check if there are statistically significant differences between the splits as shown in Fig.10. It was found out that only the new and old shutter kit is significantly different and with the wait times not showing significant differences.

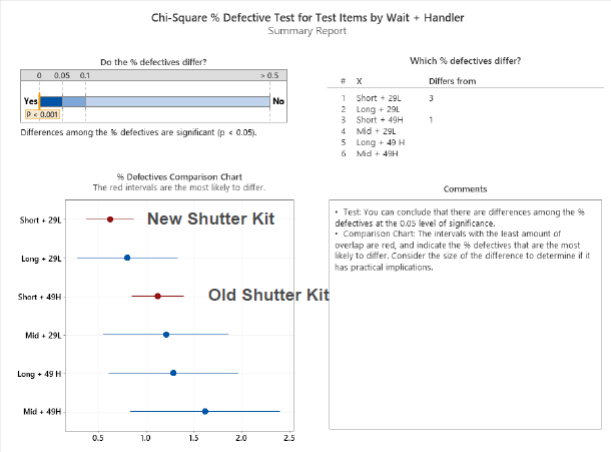

Fig.10 Chi-Square % defective for the split analysis between Shutter Kit and Shutter Control Wait time results

WhyWhy analysis was used to further check the rootcause. Table.2 shows the results.

Define Problem	Rootcause	Why1	Why2	Why3
High Yield Loss from Prox Quasi Trim and Prox Noise	Occurrence Why did it occur?	Yield loss contributed by setup with old shutter revision	Old shutter revision could not match the current speed required	Shutter kit design and limitations.
	Escapee Why was it not detected?	There was no issue / yield loss raised during test optimization implementation.	Data captured during the release may be not enough to show the long-term effect of shorter wait time and faster speeds for fan-out	
	Systemic Why was the system not able to prevent it?	The test program optimization release requirements does not cover conducting release to production lots to assess potential impact on equipment performance.		

Table.2 WhyWhy analysis for the shutter kit

3.3.4 Reference Trim table

As mentioned in 1.3 Proximity Test Parameters, individual parts are calibrated. To accomplish this, the Proximity pre-trim data is measured *(ProxPulsed_Init)*. The TP then runs the Prox Quasi Trim routine to select the best possible code in order to trim the device to the target.

As shown on the scatter plot on the left of Fig.11, the pre-trim data is measured in the X-axis showing values from around 200 to 550, whereas the specified trim target is 330. The limits are also shown both for X and Y axis and the failure rate is seen on the Prox quasi trim where units are below the lower limit.

Moreover, the scatter plot on the right of Fig.11 shows pre trim data and the coarse quasi trim colored by the available trim codes. The plot shows the trim codes above the 350 pre-trim data (X-axis) produces a bimodal distribution where most of the fails come from.

These data shows that parts with prox pre-trim values more than 450 are not being trimmed to the target consistently. As an example, a part with a prox pre trim of 500 should be trimmed down to 350, but instead it was further trimmed down to 220! While not all of the units showed the same, this mean something is wrong with either the trimming or the trim table reference.

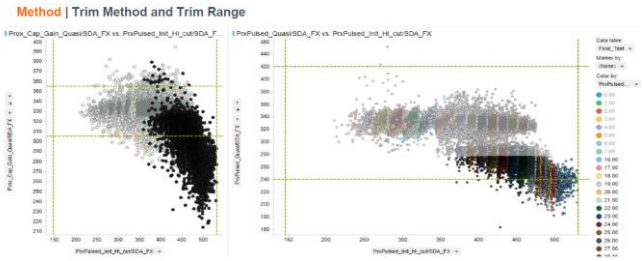

Fig.11 Scatter plot of the Proximity pre-trim data vs the Prox quasi trim and the available trim codes.

To further check on the rootcause, WhyWhy analysis with experts was conducted. Table.3 shows the results.

Define Problem	Rootcause	Why1	Why2	Why3
High Yield Loss due to Prox Quasi Trim	Occurrence Why did it occur?	Units with high initial proximity value were not trimmed properly	The current reference trim table was not able to fully cover higher proximity value range	The reference trim table was set during development phase using samples available at that time.
				There is an increase on vcsel output power on the latest vcsel batches which was not observed during development and rampup phase.
	Escapee Why was it not detected?	Safe launch lot did not show yield loss to trigger detailed analysis	The lot/s used did not include sufficient number of parts with high initial proximity value to optimize	
	Systemic Why was the system not able to prevent it?	Only available parts during development is being used which may not include edge samples to define the whole trim range.		

Table.3 WhyWhy analysis for the Trimming and Trim Table

3.4 Improve Phase

After assessing the factors, the two potential causes related to material (x_1 ASIC and x_2 VCSEL) were considered out-of-scope of the project since they are both well within the specified limits of their individual processes.

Material

x_1 ASIC Low MIM Cap sensitivity caused by higher oxide thickness (within Fab process window).

x_2 VCSEL increased Output power (within Fab process window).

Further analysis by conducting DOEs and Split analysis were considered but will not be covered in this paper.

The other two factors (x_3 Shutter Kit Design and x_4 Reference Trim Table) will proceed for improvement.

Machine

x_3 Shutter kit design

For the shutter kit design, the team has refurbished new shutter kits and the performance further checked. Fig.12 shows the significant difference in terms of yield after checking with Chi-Square % Defective Test

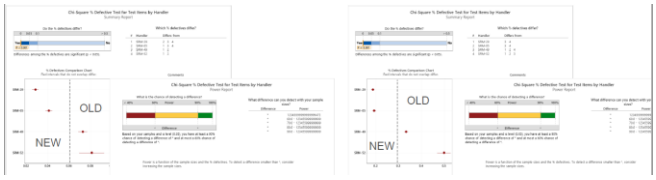

Fig.12 Chi-Square % Defective Test comparing New and Old shutter kit

Method

x_4 Reference Trim table

For the reference trim table, low and high proximity pre-trim parts were taken and using these samples the reference trim table was re-evaluated and optimized to cover the whole range of pre-trim data. Fig.13 shows the result after optimization.

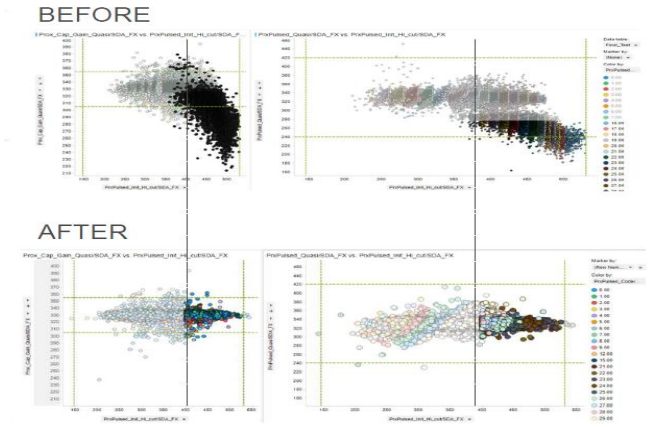

Fig.13 Before and After result of the reference trim table optimization

Bimodal distribution is no longer observed and parts more than 450 are now being trimmed down to the target.

The yield before and after the reference trim table was also checked as shown on Fig.14 and observed a significant improvement on yield from 96.3% to 98.4% and CPK from 0.19 to 4.46 on the 4 lots checked.

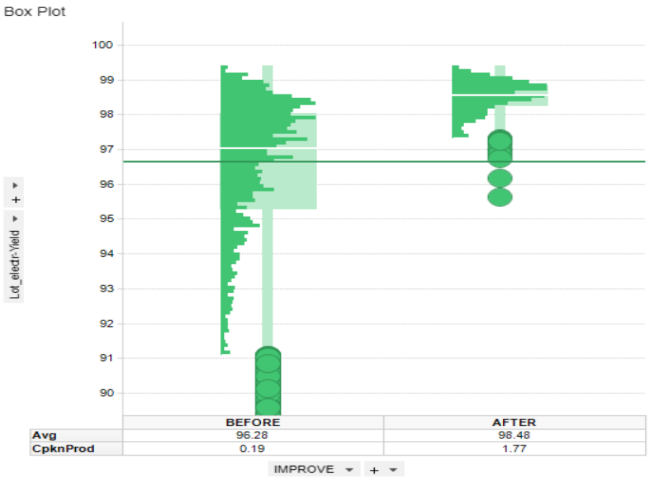

Fig.14 Yield and CPK comparison between before and after reference trim table update

3.4 Control Phase

As part of the control, the reference trim table update and test program release data were stored on the database for reference.

The yield performance is regularly being reported and reviewed during weekly meetings.

Refurbishment of new shutter kits and allocation for the device are being tracked by responsible teams.

4.0 RESULTS AND DISCUSSION

After the implementation of improvements for the shutter kit and reference trim table, the results were monitored for 3 months.

The improvements had shown good results and the targets were achieved as shown on Fig.15. with average yield from 96.28 to 98.48 and Cpk from 0.19 to 1.77.

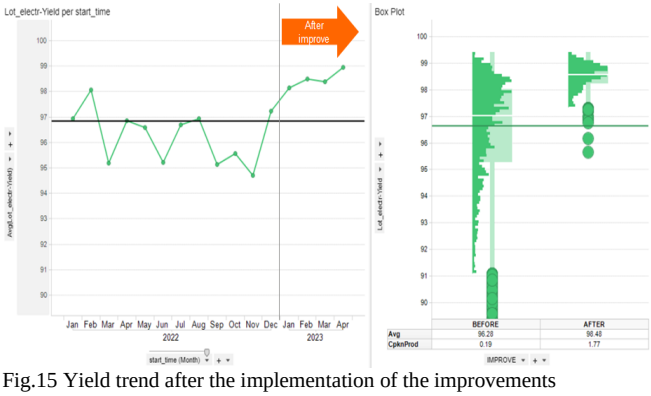

Fig.15 Yield trend after the implementation of the improvements

5.0 CONCLUSION

Through the improvement items implemented, the target yield improved by 2.4% which had a great impact in terms of cost and productivity.

The analysis and findings can be utilized as a guide for other yield improvement project plans and for new projects.

6.0 RECOMMENDATIONS

It is recommended that the results are shared to relevant teams working on similar devices as part of lesson learned for new project development. Since some factors were not considered on this project, it is also recommended to do a separate study on the other factors to avoid similar occurrence for future products.

7.0 ACKNOWLEDGMENT

The support provided by all members of the 6sigma project including the support group is greatly acknowledged by the authors. The result could not have been achieved if not for the dedication to identify the root cause and provide improvements.

Also, the authors would like to acknowledge the mentorship provided by Dr. Wolfgang Nichtl-Pecher (MBB) and Ms. Annalyn Erni (BB).

8.0 REFERENCES

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Joseph P. Panganiban, Lean 6Sigma Project “Device T Electrical Yield Improvement”, Test Quality Engineering Department, ams OSRAM Group, 2022-2023

9.0 ABOUT THE AUTHORS

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10.0 APPENDIX