ACCELERATING TEST CAPACITY THROUGH SELECTIVE POWER REGULATION AND PULSE SETTINGS OPTIMIZATION

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ABSTRACT

The primary goal in LEAN manufacturing industry is to produce high-quality but low-cost products. Most cost reduction activities for Final Test focus on Tester efficiency improvements such as Test Time Reduction activity.

In RF Final Test, Wideband Code Division Multiple Access (WCDMA) test sequence has the highest test time amongst other sequences. After further drilled down into its several components, it reveals that power regulation contributes the 75% of the WCDMA test time and only 25% consists of the actual measurement. Hence, reducing the power regulation time can significantly improve the test time. In addition, optimization on average number of pulses settings on pulse measurement was also introduced to aim the target test time reduction.

After implementation of the actions for Test Time Reduction, with the combination of two test methodologies, was able to deliver ~30% test time improvement and significantly improved the Test capacity.

This paper presented an effective structural solution thus achieving 100% yield over 20K pcs tested. This shows a good and stable performance.

1. 0 INTRODUCTION

With the evolution of technology in the field of RF Power, several semiconductor companies started to focus in transforming their business into a "Lean business".

In support of the company's Cost Reduction program, the team focuses to improve tester efficiency RF Final Test in terms of proactively improving test capacity.

In the case of Device A, the actual test time prior test improvement was high as shown in Fig 1a. Enough to affect the capacity and cost per unit of the device.

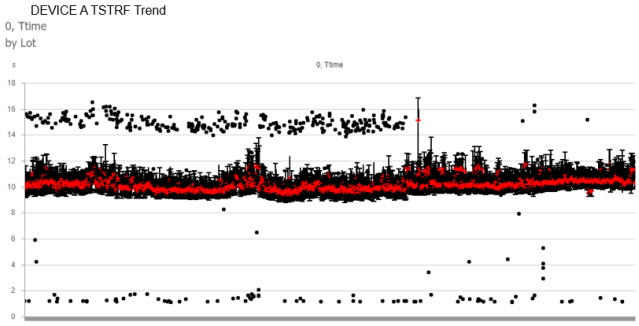

Fig 1a. Actual test time

Driven by focus on Cost Reduction program, the authors initiated to develop structural control solution through test time improvement using the existing test program without impeding the quality at Final Test.

2. 0 REVIEW OF RELATED WORK

The programming language Keysight Vee was used to create the present measuring application. This language was used to design all the measurement procedures.

Updates on the current software are made locally by a group with expertise and experience in relation to development and routine adjustments for concepts that were originally developed locally. Additionally, ongoing communication and consultations with the Nijmegen-based program developer to keep them updated on the project's development.

3.0 METHODOLOGY

2.1 Power Regulation Levelling

In Power Regulation Levelling, the concept is that the required output power is the same for the full output power levelling. This process of levelling will only be done in the following cases: (1) First sample in the tested batch. (2) Upon

parametric reject encounter. (3) Middle of the batch (4) Resulting output power not within the required output power tolerance as shown in fig 1.

For the other good devices on the same batch, signal generator power will be the average value of all used levels in a batch.

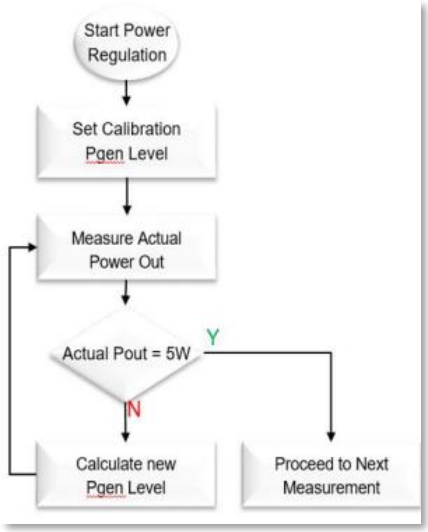

Fig 1. Power Regulation Concept

2.2 Average Number of Pulse settings

In the early releases of test program, AUTO is the default averaging setting in CW_Pulsed sequence. Default calculation of AUTO averaging: *1024/((pulsewidth-20u)/10u)*
(for PdB and power sweep sequence: *512/((pulsewidth-20u)/10u)) Example with 100u pulse width: 1024/((**100u**-20u)/10u)=128steps*

We then introduced different selection in the averaging count of CW_Pulsed measurement. The program is flexible to different calculated averaging selection as shown in Fig 3.

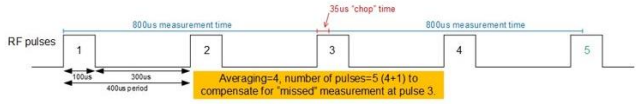

Fig2. CW Pulsed signal

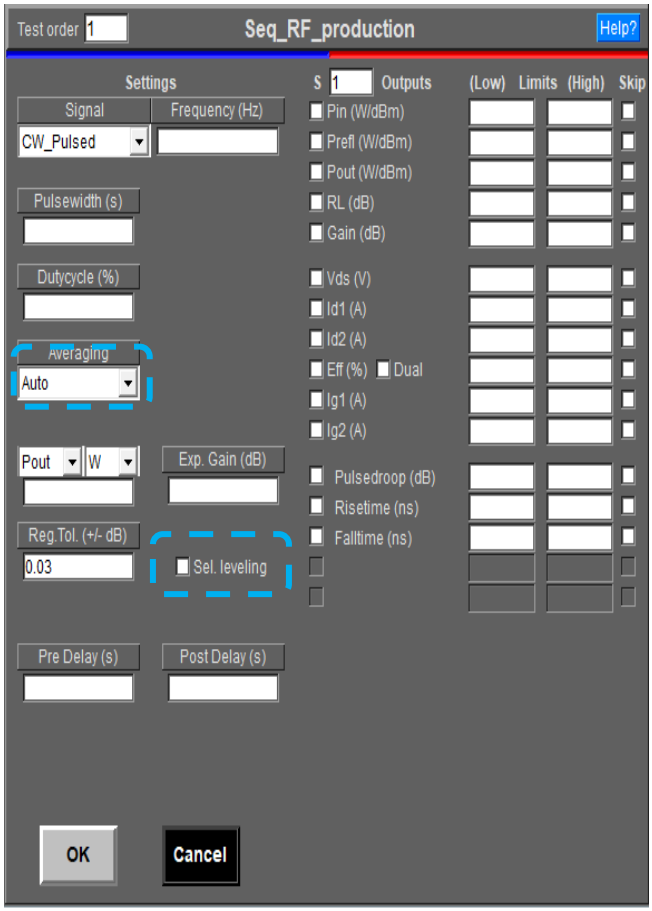

Fig 3. Program update for Averaging and Power Regulation Levelling

4.0 RESULTS AND DISCUSSION

The concept grants that input power will be used on the following samples in case the resulting output power is within the required tolerance. As shown in Fig 4, DUT1 did a power levelling and achieved a power generator level of -12.1 in ~0.5s sequence time. Applying power regulation levelling, on the next DUT, it used the previous power generator level and achieved a Pout that is within the tolerance. The process on the next DUT only acquired ~0.15s instead of ~0.5s.

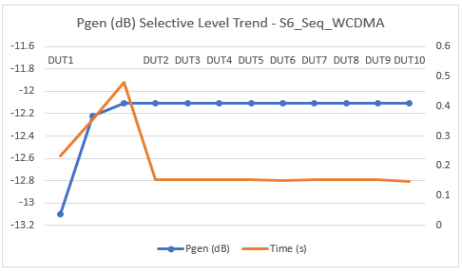

Fig 4. Power Generator Level versus Test time per Device

An initial study was done to see the measurement result of different averaging values. Measurement accuracy improves with increasing averaging. The study shows that averaging relatively affects the test time. Thes result confirms that averaging at 32, 64, and 128 has comparable values as shown in Fig 5.

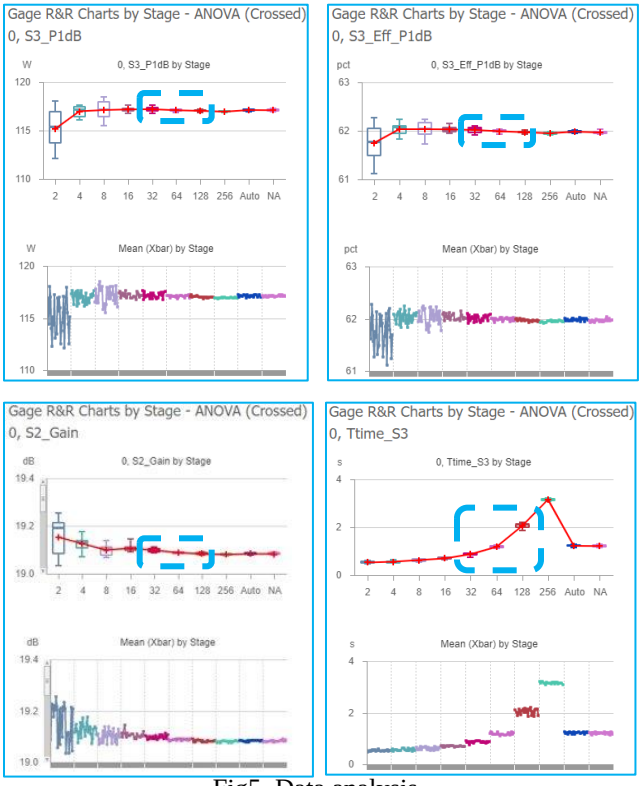

Fig5. Data analysis

A Measurement System Comparison (MSC) was performed to compare the measurement result of the conventional method and Power Regulation Levelling test method as shown in figure 6. Total R&R is still acceptable. The shift difference on the parameters is still well within the acceptable correlation tolerance as shown in Fig 7.

Parametric test				%Study var		Dist.	%Tol (6 * stdev / tolerance)				
Test name	Unit	LSL	USL	Gage R&R	Part-Part	cat.	Reprod. (AV)	Repeat. (EV)	Repeat. Old TP	Repeat. Selective Levelling	Total R&R
S2_ACPR_5M	dBc	-45.00	-25.00	37.66	92.64	3	0.94	2.85	1.74	3.64	3.00
S2_Eff	pct	49.30	65.00	50.39	86.38	2	3.59	12.53	14.07	10.76	13.03
S2_Gain	dB	15.30	18.50	56.40	82.57	2	10.44	10.53	9.69	11.31	14.83
S2_RL	dB	6.50	30.00	46.46	88.55	2	4.73	9.41	6.73	11.49	10.54
S3_ACPR_5M	dBc	-45.00	-25.00	36.29	93.18	3	1.50	3.64	2.20	4.65	3.94
S3_Eff	pct	49.30	65.00	47.12	88.21	2	2.06	9.22	9.52	8.91	9.45
S3_Gain	dB	15.30	18.50	42.51	90.51	3	9.55	9.52	8.10	10.76	13.48
S3_RL	dB	6.50	30.00	36.65	93.04	3	4.79	8.47	6.05	10.34	9.74

Fig 6 MSC results for main parameters

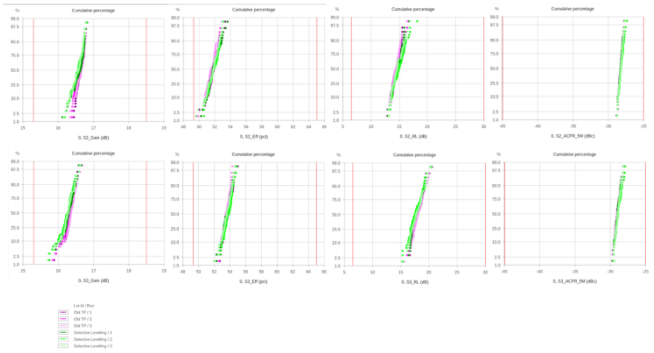

Fig 7 MSC Parameter trend on each run for the main parameters

5.0 CONCLUSION

After implementation of the agreed actions, test time was improved to ~30% test time reduction through the combination of new test methodologies – Power Regulation levelling and average number of pulses settings optimization. In which, significantly improved Test capacity and cost reduction per unit.

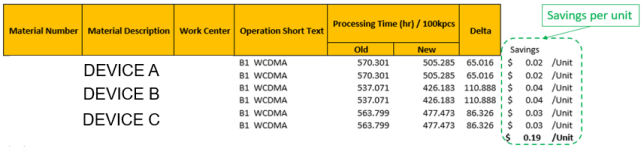

Fig 8a Actual savings calculation

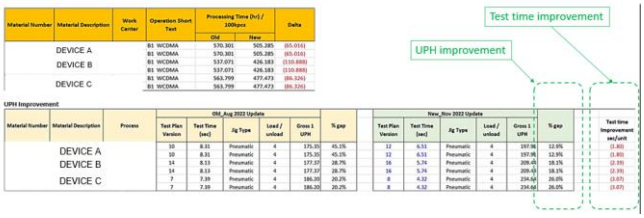

Fig 8b Actual savings calculation

Initial positive result was observed on the released product. The RF test yield is 100% over 20K pcs tested. This shows a good stable performance. All critical RF parameters have > 1.0 Cpk.as shown in Fig 9.

Parametric test			Limits		Part statistics			Test yield	
Test number	Test name	Unit	Low limit	High limit	Mean	Cp	Cpk	Result count	Yield (%)
0	S2_ACPR_5M	dBc	-45	-25	-28.027	6.39	1.934	20094	100.0
0	S2_Gain	dB	15.3	18.5	15.951	2.614	1.064	20094	100.0
0	S2_RL	dB	6.5	30	9.827	3.784	1.071	20094	100.0
0	S3_ACPR_5M	dBc	-45	-25	-30.376	4.633	2.49	20094	100.0
0	S3_Gain	dB	15.3	18.5	16.178	2.304	1.265	20094	100.0
0	S3_RL	dB	6.5	30	14.82	2.199	1.557	20094	100.0
0	S5_P3dB	W	400.0	600.0	501.3	1.371	1.352	20094	100.0
0	S7_P3dB	W	400.0	600.0	494.5	1.162	1.098	20094	100.0

Fig 9 Test Results from production lots

6.0 RECOMMENDATIONS

Implement the test methodologies on the new incoming device types and fanout to all released packages with optimum number of pulses and Power Regulation levelling based on device capability after thorough analysis.

7.0 ACKNOWLEDGMENT

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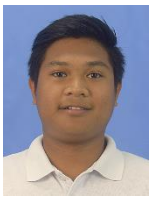
8.0 REFERENCES

1. RF Transistors Parameter Measurement Procedure, MST Base Stations.
2. RF Testing in Manufacturing, Paul Schaffner
3. Angus, Robert B., and Thomas E. Hulbert. VEE Pro: practical graphical programming; [includes VEE 7.0 features]. Springer Science & Business Media, 2005.

9.0 ABOUT THE AUTHORS



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